Journal of Scientific Research and Development 3 (3): 47-51, 2016
Available online at www.jsrad.org
ISSN 1115-7569

Development of Cockcroft-Walton voltage multiplier for RF energy harvesting applications

E. M. Ali, N. Z. Yahaya *, N. Perumal, M. A. Zakariya[4]

Department of Electrical and Electronic Engineering, University Teknologi PETRONAS, Bandar Seri Iskandar, 31750 Tronoh, Perak, Malaysia

Abstract: The Cockcroft-Walton voltage multiplier circuit is designed from a series of rectifiers to obtain high DC voltage. In the presented model, the DC voltage, which is generated in the present stage, contributes to a higher value in the next stage. Every stage produces a higher DC output voltage. The proposed signaling scheme enables the use of the rectified DC voltage in a classical way along with the involvement of instantaneous RF input voltage. In this paper, a seven-stage Cockcroft-Walton voltage multiplier is used. The design was optimized via simulation based on Schottky diode HSMS 285C. It was enhanced utilizing Advanced Design System (ADS) 2009, while the prototype was fabricated on RT/ Duroid 5880 (RO5880) printed circuit board (PCB) substrate with dielectric constant and loss tangent of 2.2 and 0.0009 respectively. Experimentally, the output voltage is found to be 6.47 V harvested from the operating frequency of 900 MHz within board dimensions of (45x19x1.57) mm in addition to sufficient DC current level. Hence, this is suitable for battery charging applications.

Key words: Cockcroft- Walton; Voltage multiplier; RF harvester; GSM 900 MHz, Mobile charging

1. Introduction

The rectifier is a device which converts RF signal received through antenna into a suitable DC supply voltage. It includes charge pump, Villard voltage Doubler and Cockcroft-Walton voltage multiplier (Everhart and Lorrain, 1953). The voltage multiplier converts part of incoming power supply to DC. A DC voltage of twice the peak amplitude of the alternating current (AC) signal can be generated at the DC output terminal. Fig. 1 shows basic circuit of charge pumps constructed using two diodes and two capacitors (Patel and Dave, 2013).

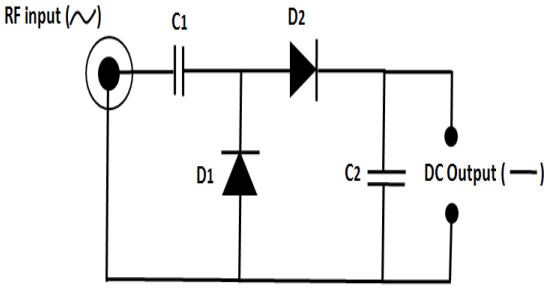

Fig. 1: Single stage of voltage multiplier

When a number of *n-stage* of these circuits are tied together in series and connected to the load as shown in Fig. 2, the output voltage gained given by this change in DC value will make the time constant longer.

$$V_{out} = \frac{nVo}{nR_L+Ro} R_L = Vo \frac{1}{\frac{Ro}{R_L}+\frac{1}{n}} \quad (1)$$

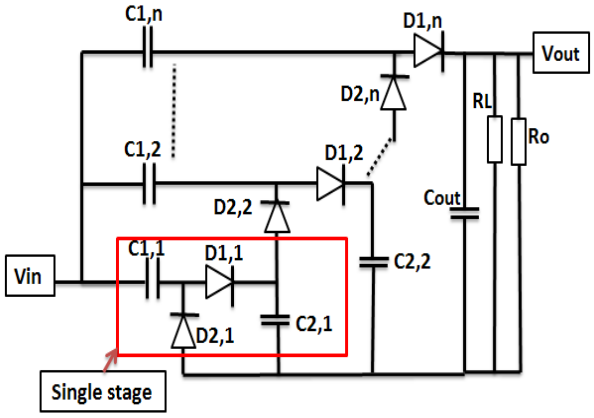

Fig. 2: N-stages of voltage multiplier

Where, *Vo* is the open circuit voltage, *Ro* is the internal resistance, R_L is the load resistance and *n* is the number of stages. Hence, the number of stages in the system has the greatest effect on the DC output voltage, as given in Eq. 1 (Hucheng, 2014) and (Harrist, 2004).

The design of voltage multiplier circuit has been presented in various literatures as listed in Table 1. This includes the recent projects in the development and application of voltage multiplier circuits. This work focuses on designing, testing and measuring a seven-stage Cockcroft-Walton voltage multiplier using harmonic balance method as a function of an AC to DC converter, which rectifies the input AC

* Corresponding Author.

signal and increases the DC voltage level at GSM 900 MHZ frequency band.

Table 1: Recent advances of projects on voltage multiplier

Ref.	Frequency	Number of stages	Comments
(Hart et al., 2005)	S band frequency	7 stages	The authors designed the charge pump using Schottky diode to light emitting diodes.
(Jabbar et al.,2010)	2.4 GHz	1 stage	Villard voltage multiplier is designed using technology of CMOS; efficiency of the circuit is 22.97% at 66μW input. The output voltage is 1.5 V.
(Arrawatia et al., 2010)	2.67 GHz	5 stages	Villard voltage multiplier is designed using technology of CMOS, output voltage of 1.04 V.
(Arrawatia et al., 2011)	900 MHZ	6 stages	A voltage of 2.78 V is measured at a distance of 10m from the cell tower.
(Hong et al., 2013)	2.48 GHz	7 stages	The harvested voltage is 2.3 V.
(Akter et al., 2014)	900 MHz	5 stages	The output voltage of 2.5 V, output current of 25μA.
(Esraa et al., 2014)	900 MHz	3 stages	A generator of 3-stage voltage multiplier is designed using balance harmonic method. Every stage is designed with/without the matching circuit. The value of the output voltage after adding the matching circuit is 6.355 V.
(Esraa et al., 2015)	900 MHz	3 stages	Villard voltage doubler circuit is designed and simulated by Advanced Design System (ADS) software. This circuit is optimized and achieved by using Schottky diode pair HSMS-285B.

2. Methodology

The design of the voltage multiplier is illustrated by the block diagram in Fig. 3. It shows the process in designing a seven-stage Cockcroft-Walton voltage multiplier from literature findings to the actual in-lab scale implementation. Once a clear understanding on the existing technologies of subject matter is perceived, then a new proposed technique will be developed based on all advantages and limitations referred in literatures. Later, the work will be simulated to look for correct algorithm in introducing a new systematic way to produce a better RECTENNA design. Then, the hardware circuit is constructed to justify the analyses via experimentation.

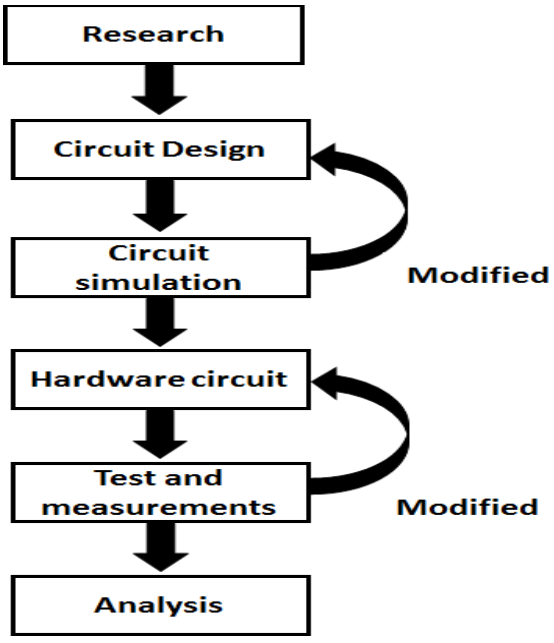

Fig. 3: Block diagram of the methodology

3. Simulation setup

3.1. Design of Cockcroft-Walton voltage multiplier

The design has to carefully consider correct selection of components. All values are referred to specific calculations. As for the capacitors, they are inversely proportional to the frequency of the input signal. This means if the value of the input frequency is 900 MHZ, the value of the capacitors will be in range of pico Farads.

The Cockcroft-Walton multiplier circuit utilizes a Schottky diode HSMS 285c. Upon choosing this component, the output voltage across the load decreases during the negative half cycle of the AC input signal. The voltage is inversely proportional to the product of resistance and capacitance across the load. Without the load resistor in the circuit, the voltage would be held indefinitely in the capacitor and look like a DC signal, assuming it is an ideal component. The capacitors are then charged to the peak value of the input RF signal and discharged to the series resistance (R_s) of the diode.

Thus, the output voltage across the capacitor in the first stage of multiplier is approximately twice that of the input signal. As the signal swings from one stage to another, there is an additive resistance in the discharge path of the diode and increase of capacitance due to the stage capacitors (Akter et al., 2014).

In the design of multiplier circuit, it is very essential to calculate the voltage regulation and percentage ripple (Devi et al., 2012). Based on Eq. 2, the output voltage is measured based on the number of cascaded multiplier which indeed will raise the output voltage level.

$$V_{out} = (2 \times N \times V_{max}) - \Delta V - \delta V \quad (2)$$

Where, V_{out} = output voltage of N stage voltage multiplier, N = no. of stages (it is number of capacitor divided by 2), V_{max}= maximum or peak input voltage, ΔV = resultant drop across the capacitors and δV = ripples voltage (peak to peak).

When the load is connected, the resultant voltage will drop across capacitors. This will influence the effective current generation and also voltage ripple. The voltage load fluctuation is given in Eq. 3.

$$\Delta V = \left(\frac{1}{f \times C} \times \left\{\left((2 \times n^3) \div 3\right) + (n^2 \div 2) - (n \div 6)\right\}\right) \quad (3)$$

The ripple voltage δV (peak to peak) can be calculated using Eq. 4 with its respective regulation and percentage are given in Eq. 5 and Eq. 6 respectively.

$$\delta V = \left(\frac{1 \times n \times (n+1)}{4 \times f \times C}\right) \quad (4)$$

$$\text{Regulation of Voltage} = \Delta V / 2V_{max} \quad (5)$$

$$\text{Percentage Ripple} = \delta V / 2V_{max} \quad (6)$$

When load is not connected, δV and ΔV both are zero thus the above equation is reduced to Eq. (7).

$$V_{out} = 2 \times N \times V_{max} \quad (7)$$

3.2. Simulation of Cockcroft-Walton voltage multiplier

The ADS simulator 2009 is used to simulate the seven-stage Cockcroft-Walton voltage multiplier as shown in Fig. 4. It contains a combination of capacitors and diodes which were carefully conFig.d and selected in the design. The AC signal is first fed into the input side where it will channel into the cascaded block of multiplier stage. In each stage, the voltage will be converted into DC and this gradually increases the value up to higher level as long as load current does not reach zero. Due to this fact, the inability to get required load current, having an increase in voltage, will hamper the potential in getting the correct signals to charge the mobile application.

Fig. 5 shows the results of simulation of the seven-stage voltage multiplier circuit without a matching circuit. The m3 line illustrates the AC input signal and m4 line illustrates the DC output captured at the output-end of rectifier. It shows that the input voltage is 1.060 V (first stage) with the output voltage of 4.525 V (seventh stage). However, this output voltage does not yet achieve required value at 5 V minimum for the charging potential. Therefore, the design has to include matching circuit to ensure an increase level in output voltage.

Interestingly, Fig. 6 shows the simulation results of the voltage multiplier after adding the matching circuit. Interestingly, the output voltage level has increased to 5.866 V (seventh stage), hence sufficient for mobile phone battery charging application. Nevertheless, as DC load voltage increases, the effective conducting DC current will eventually decreases. Thus, the design will be required to look into better option in order to increase the current while maintaining the 5-V potential at the load. In this case, the current amplifier circuit is adopted in the design as shown in Fig. 7. Even though the DC current is low, for example 25 mA at 5 V, the battery will need a longer time to charge to its maximum level compared to 1 A, which indeed not a good sign of achievement.

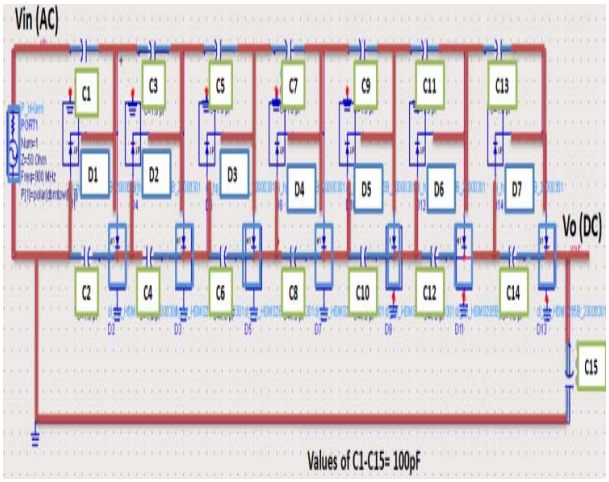

Fig. 4: Seven-stage voltage multiplier

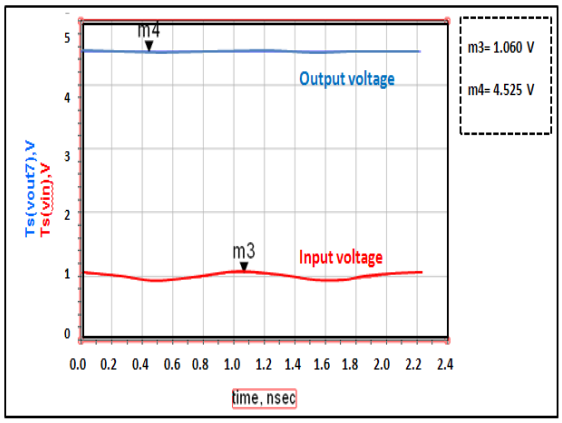

Fig. 5: Simulation result of seven- stage voltage multiplier circuit before adding matching circuit

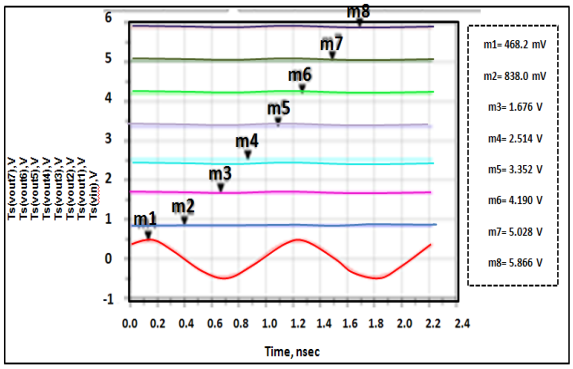

Fig. 6: Simulation result of seven- stage voltage multiplier circuit after adding matching circuit

Fig. 7 shows the current amplifier circuit consisting of several transistors, resistors, capacitor and Zener diode. The initial input DC current will be fed through R_2 in which it will be amplified in accordance to a certain gain of transistor at the load measured at the probe. During the amplification stage, the DC voltage level is monitored closely and should it result in any decrement due to the

increment of DC current level, C_{17}, R_3 and R_4 are recalculated and adjusted. Therefore, the DC voltage level will be managed effectively to a required level close to 5 V.

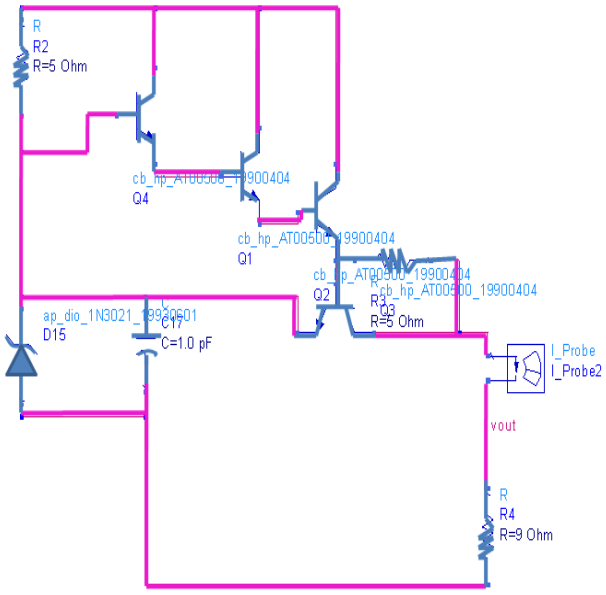

Fig. 7 : Curent amplifier circuit design

Fig. 8 and Fig. 9 show the simulation results for both current and voltage measured upon combining Cockcroft Walton multiplier voltage circuit with amplifier current circuit. It can be seen that the output current has increased from 0.25 mA into 565 mA, which is now good enough to charge the battery of mobile phone and furthermore the time taken to charge increases by more than 97 % from the initial 13 mA. However, the respective DC voltage load has dropped slightly from 5.866 V to 5.081 V. Here the measured values are acceptable to represent charging voltage level based on the applicable physical battery unit used by the phone.

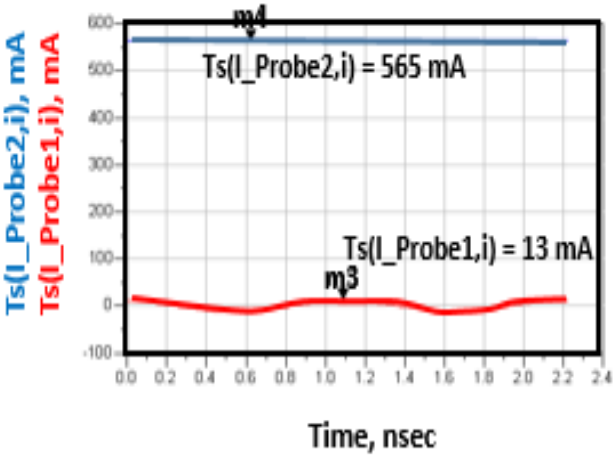

Fig. 8: Simulated output current of regulated Cockcroft-Walton voltage multiplier

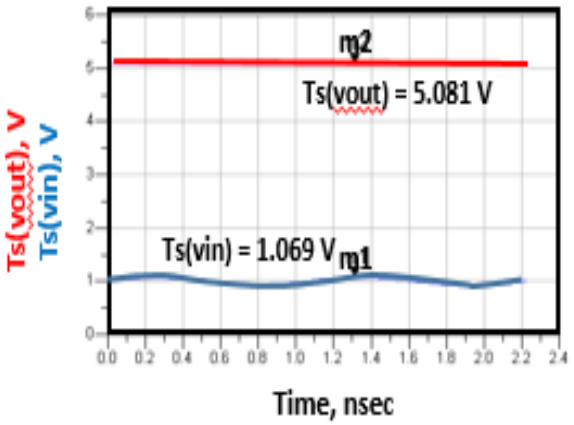

Fig. 9: Simulated output voltage of regulated Cockcroft-Walton voltage multiplier

3.3. Prototyping of Cockcroft-Walton voltage multiplier

The prototyping of the rectifier starts with the conversion from ADS file to Eagle, the PCB schematic block. Here the dimension of the rectifier is limited to only 45 mm by 18 mm.

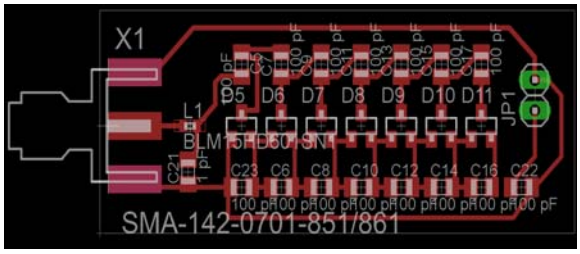

Fig. 10: Seven stages rectifier simulated using PCB Eagle software

Fig. 10 clearly shows the orientation of component footprints in the PCB fabrication stage. The SMA connector is labelled as X1. The rest of the components are being arranged carefully in accordance to the design rule check (DRC) governed by the software. The actual physical fabricated unit of the rectifier is illustrated in Fig. 11. It is fabricated on RT/Duroid 5889 (RO5880) substrate with dielectric constant and loss tangent of 2.2 and 0.0009 respectively.

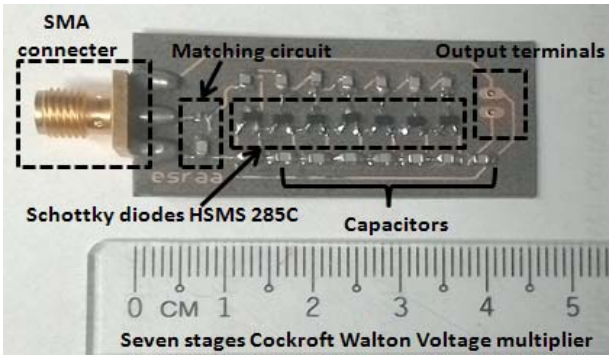

Fig. 11: Prototype of seven stages Cockcroft Walton voltage multiplier

4. Results and discussion

Fig. 12 shows the measurement setup to test and measure the design using RF generator, Cockcroft-Walton voltage multiplier circuit and multi meter. The RF generator delivers the RF signal to the rectifier at 900 MHz which is connected using coaxial cable. The multi meter is attached to the terminals of the rectifier to test the output voltage. From the results, it is surprised to see that output voltage is 6.47 V which is slightly higher than the expected 5 V or even in simulation, 5.886 V. This is due to the matching circuit which may require some adjustments to achieve the required potential. As for the current, it still manages to cap at around 550 mA.

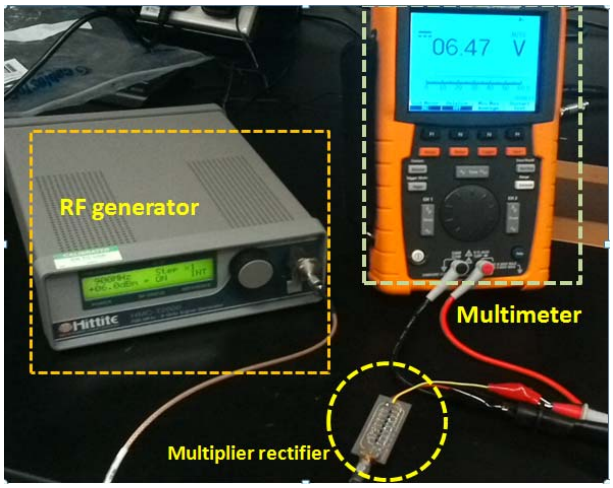

Fig. 12: Test and measurement of seven-stage Cockcroft-Walton voltage multiplier

5. Conclusion

In this paper, a seven-stage Cockcroft-Walton voltage multiplier is designed at 900 MHz. It is simulated using Advanced Design System (ADS 2009). The design is fabricated using Roger 5880 board of 2.2 dielectric constant and 1.6 mm thickness giving an output voltage of 6.47 V. Even though the measured result is higher than simulated, this can be further adjusted to achieve 5 V as required for the battery charging module. From the work, it can be concluded that the newly designed rectifier is able to convert the captured RF power into DC load voltage with better results.

Acknowledgement

Authors are gratefully acknowledging the Ministry of Higher Education (MOHE) of Malaysia for financial support in completing the work using Fundamental Research Grant Scheme (FRGS). Thanks to all other personnel especially Mr. ADZ and Mr Azwan, lab technologist, by sharing their efforts in the testing and measurement skills. Lastly, to Dr. Shahid Iqbal from Universiti Sains Malaysia for his assistance in giving beneficial ideas towards formulation in the design.

References

D. W. Harrist, (2004). "Wireless battery charging system using radio frequency energy harvesting". M.S. Thesis, University of Pittsburgh, Pittsburgh.

E. Everhart, and P. Lorrain, (1953). "The Cockcroft–Walton multiplying circuit". Rev. Sci. Instrum. 24: 221–226.

E. M. Ali, N. Z. Yahaya, N. Perumal and M. A. Zakariya, (2014), "Design of RF to DC rectifier at GSM band for energy harvesting applications", A Journal of Engineering, Science and Society, 10(2): 15-22.

E. M. Ali, N. Z. Yahaya, N. Perumal and M. A. Zakariya, (2015), "Design and development of harvester RECTENNA at GSM band for battery charging applications", Journal of Engineering and Applied Sciences, 10(21): 10206-10212.

H. Hart, K. Lanham and M. Sass, (2009). "S-band radio frequency energy harvesting". Science Applications International Corporation.

H. Jabbar, S. S. Young and T. J. Taikyeong, (2010). "RF energy harvesting system and circuits for charging of mobile devices". IEEE Transactions on Consumer Electronics. 56(1): 247-253.

K. K. A. Devi, M. D. Norashidah and C. K. Chakrabarty, (2012), "Optimization of the voltage doubler stages in an RF-DC convertor module for energy harvesting", Circuits and Systems. 3: 216-222.

M. Arrawatia, M. S. Baghini and G. Kumar, (2010). "RF energy harvesting system at 2.67 and 5.8 GHz". Proceedings of Asia Pacific Microwave Conference, 900–903.

M. Arrawatia, M. S. Baghini, and G. Kumar, (2011). "RF energy harvesting system from cell towers in 900 MHz band". National Conference on Communications. 28–30.

N. Akter, B. Hossain, H. Kabir and A. H. Bhuiyan, (2014). "Design and performance analysis of 10-stage voltage doublers RF energy harvesting circuit for wireless sensor network". Journal of Communications Engineering and Networks. 2(2): 84-91.

P. S. Patel and D. B. Dave, (2013). "Design, analysis and implementation of negative high voltage DC power supply using voltage multiplier circuits". International Journal of Engineering Trends and Technology. 4(4): 702-706.

S. Hucheng, (2014). "Design and analysis of antennas and rectifying Circuits for wireless power transmission and ambient RF energy harvesting". Thesis of PhD. University of Science and Technology of China.

S. S. B. Hong, R. Ibrahim, Khir H. M. M., M. A. Zakariya and H. Daud, (2013). "WI-FI energy harvester for low power RFID application. Progress in Electromagnetics Research C. 40: 69–81.