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Analysis and simulation of carbon Nanotubes structure and application CNT on the based circuits and their introduction to a new low power delay flip flop

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Abstract: Carbon Nanotubes are long, hollow structures with the walls formed by one-atom thick of carbon sheets. Carbon Nanotube –based transistors which include adjacent semiconducting single-walled transistors, are a good substitute for silicone CMOS circuits due to their excellent electronic properties. Present study examines CNTFET and CMOS transistors in 32nm technology using HSPICE software. Next, flip flop circuits are studied and simulated and a new D flip flop is introduced which is used in memory ICs with a carbon Nanotube field effect transistor. Simulation results indicated a significant improvement in power, delay, noise margin and mutation in CNTFET technology compared with CMOS based technology. Results showed that, due to its lower power consumption and higher speed, CNTFET could be a good substitute for CMOS transistors.

Key words: Carbon Nanotube transistor; CNTFET; D flip flop; Basic circuits; Low power consumption; Low propagation delay

1. Introduction

Carbon Nanotubes, long thin cylinders of graphite, were first discovered in 1991 by SumioIjima of the NEC laboratory. Graphite is a common structure of carbon atoms that consists of multiple layers of carbon atoms arranged in a hexagonal lattice like a wire mesh. Although the mesh structure is by itself a strong structure, there is no chemical bond among layers and only weak von der waals forces keep them together. The layers can easily slide over each other making it soft and slippery so that it slips easily off the pencil onto the paper and leaves a black mark. Fig. 1 shows various carbon compounds found in nature (Moore, 2009).

Graphite sheets are rather flexible and by rolling up a graphite sheet into a cylinder, we have actually built a Nanotube. At the end of the tube, carbons usually bond to each other and block the Nanotube. The capping units consist of pentagons which provide the curvature necessary for closure. Because of these pentagons, Nanotubes are sometimes classified as a member of fullerene family. Fullerenes are a series of hollow carbon molecules that form a closed cage and Bucky balls are the most famous form of fullerenes (ITRS, 2009). This molecule consists of 60 carbon atoms that form the shape of a ball like a football. If you add 10 carbon atoms to the middle of a Bucky ball, you obtain another fullerene called C70 which is partly changed from spherical shape (C60) to an elliptical one. By adding another 10 atoms, we obtain C80 and by continuing this trend we can reach various carbon Nanotubes (Masoud Miri, 2006). The aim of the present study is to first give an overview of carbon Nanotubes and examine their Nano electronic related properties. Then, a detailed study of the structure and performance of CNTFET transistors is presented and their substantial differences with CMOS are expressed. Next, using a model developed in Stanford University, a new D-flip flop is simulated which is widely applied in memory circuits. Then the results of CMOS technology are compared with the results obtained from CNTFET technology. Results indicate that power consumption in CNTFET circuits is much lower than that in CMOS, while a significant improvement has also been observed in the circuit speed.

2. Comparing CMOS with CNTFET on very small scales

Since the development of first transistor in 1998, the progress of CNTFET led to a fixed improvement in electric specification that was explained in the previous section. A preliminary work was done by Martel et al (Yildirim et al., 2000) who made a comparison with the modern technology of silicon MOSFETS. Their back-gated CNTFET with source-drain contacts of Ti/TiC was able to compete with the new MOSFET (Chen et al., 2006). Upper gate transistor which was accurately designed and developed by Wind et al showed unexpected values for mutual conductance and maximum drive current (Wind et al., 2002). The presence of some special specifications in carbon Nanotube makes them an ideal choice for most applications.

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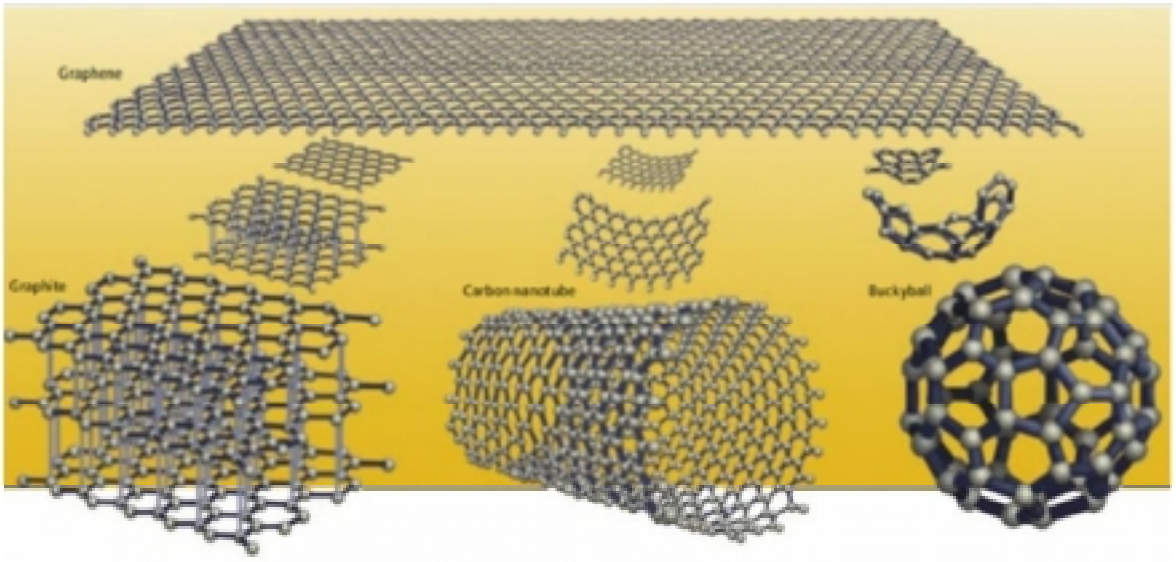

Fig. 1: Various carbon compounds found in nature (Masoud Miri, 2006)

Today the research trend about Nanotubes is mainly focused on their application in tools' structure. Most researchers working in various universities and laboratories from across the world predict that in the near future Nanotubes will be widely applied in various areas (Martel et al., 2001). Development of some interesting tools is already possible, but for commercial success, future will decide. Electrical properties and chemical stability will absolutely lead us to exploitation of these features. Thus, in the next sections characteristic curve of transistor will be discussed.

First, the characteristic curve of transistor will be extracted by the model and then VLSI basic circuits will be simulated by CNTFET. To this end, we have tried to examine effective parameters in I-V curve including number of Nanotubes, chirality of Nanotube and other factors that may be changed by designer.

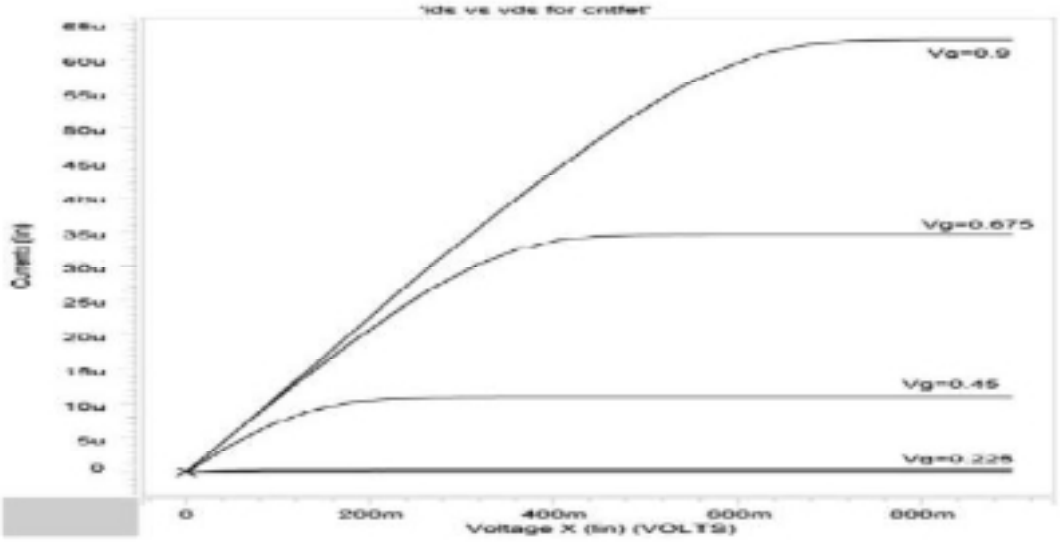

Fig. 2: Characteristic I-V curve of an n-type carbon Nanotube field effect transistor with chirality of (19, 0), 3 tubes and gate length of 32mn (Marulanda and Srivastava, 2007)

Fig. 2 shows the characteristic curve of a carbon Nanotube field effect transistor with chirality of (19,0). This characteristic has been obtained with 3 Nanotubes in the transistor channel. In fact, fig (2) shows the changes in drain current of n-type carbon Nanotube transistor vs. various gate-source voltages. As it could be seen in figs (3-5), drain current for Vgs= 0.225 is zero so it can be concluded that the threshold voltage of a transistor with this chirality and this insulation specification would be higher than this value which is consistent with the theoretically obtained value of 0.289. It is worth noting that the value of threshold voltage is obtained by the following relation.

$$E_{\cdot} \frac{\cdot}{\cdot} \quad (1)$$

$$V_{\cdot} = \frac{E_{\cdot}}{\cdot} = \frac{\cdot}{\cdot} \quad (2)$$

Where ac-c is the bond length of carbon-carbon which is equivalent to 2.49 Å, $V_{\pi-\pi}$ is π π^* binding energy of carbon which is equivalent to 3.033 ev, e is the electron charge, and DCNT is the diameter of Nanotube. The diameter of (19, 0) Nanotube is equivalent to 1.49 nm. Fig. 3 shows the I-V characteristic curve of a CMOS transistor for 32nm technology.

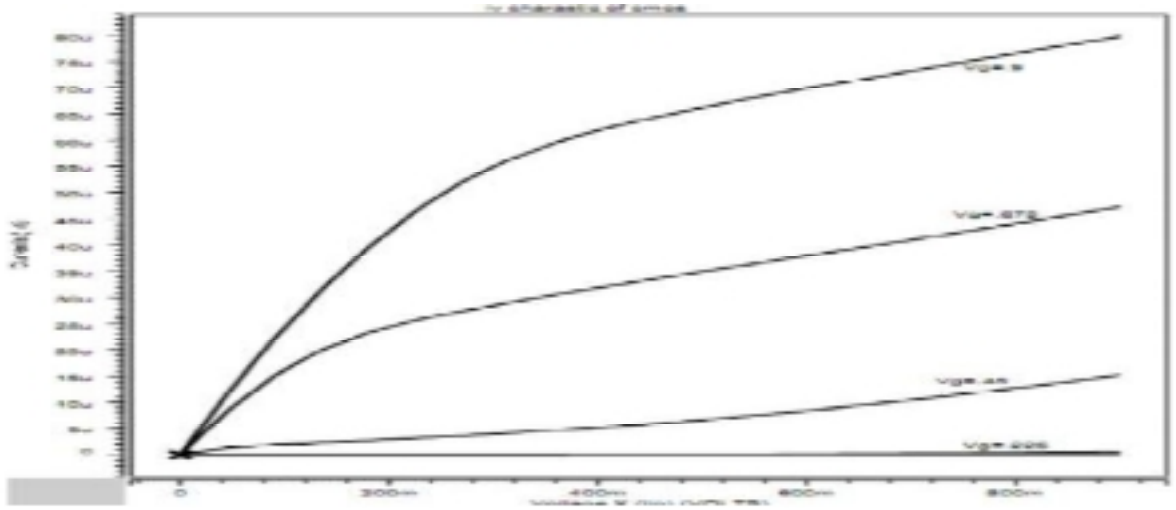

Fig. 3: I-V characteristic curve of CMOS transistor in 32nm technology for various gate voltages (Marulanda and Srivastava, 2007).

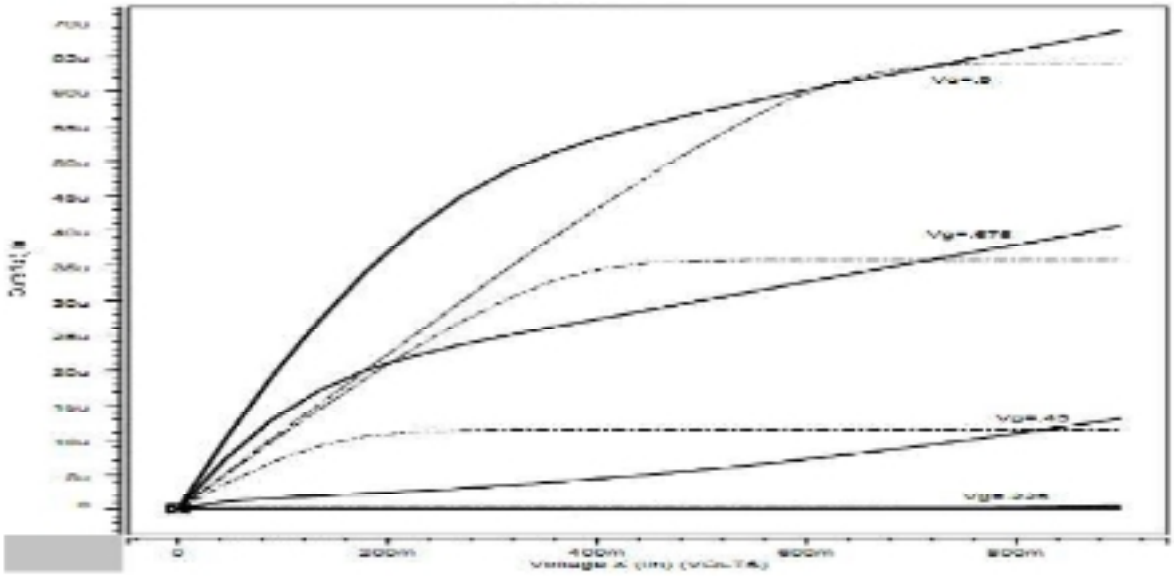

Fig. 4: I-V characteristic curve of CMOS transistor in 32nm technology with gate width of 112 nm (solid lines) and I-V characteristic curve of CNTFET transistor with 3 Nanotubes in the channel (dashed line) (Marulanda and Srivastava, 2007).

According to Fig. 4 it is clearly obvious that gate voltage of 0.225 is not enough to operate CMOS transistor in 32nm technology and higher voltages are required. In Fig. 4 characteristics of n-type transistor in two technologies are shown on a coordinate plane. In this simulation, the transistor channel width of 3.5 Nmos is equivalent to its gate length and a number of 3 Nanotubes has been chosen in the channel of carbon Nanotube transistor. In this case, transistor width NMOS will be equal to 112nm while in CNTFET case this value is 60 nm. Since the step value of 20 nm and the number of 3 Nanotubes have been chosen in this simulation, the gate length of 32nm is applied for both technologies. By detailed examination of I-V curve it could be clearly seen that slope of the curve for CMOS technology in the saturation region is higher than that for CNTFET technology. In higher drain voltages, this slope makes NFET transistor to have higher maximum output current. But in lower voltages of gate and drain, CNTFET outperfomes CMOS. It is worth noting that increasing the number of Nanotubes in CNTFET transistor entails higher drain current that is shown in Fig. 5. For example, with 7 Nanotubes and in the saturation border, drain current will be 1.10^{-4} which is an acceptable value and is located at the upper area of NFET curve.

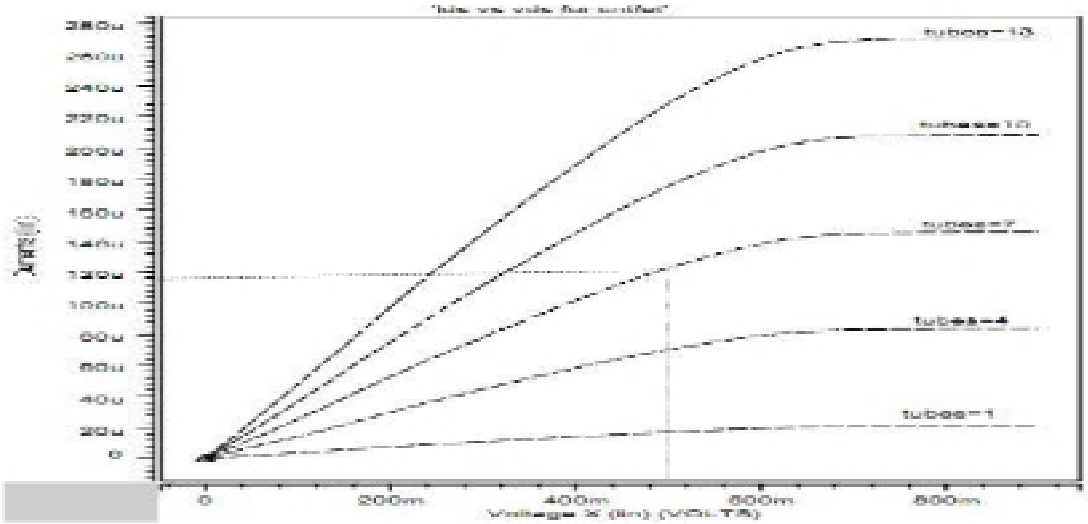

Fig. 5: I-V characteristic curve of a carbon Nanotube field effect transistor in terms of changes in Nanotubes number and vsg=0.9 (Marulanda and Srivastava, 2007).

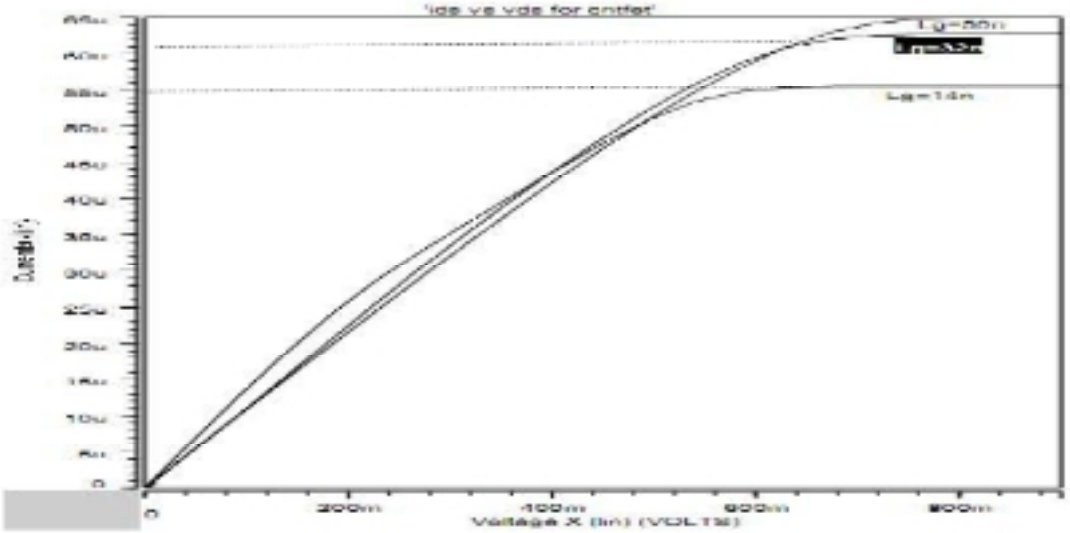

Fig. 6: I-V characteristic curve of a carbon Nanotube field effect transistor in terms of various gate lengths and vgs = 0.9 (Marulanda and Srivastava, 2007).

Fig. 6 shows the I-V curve of a CNTFET transistor for 3 different gate lengths. It could be observed that for gate length of 14 nm, drain current is equivalent to [illegible], while for gate length of 32nm, this current reaches [illegible]. But for gate length of 50 nm, drain current shows only a [illegible] increase and reaches [illegible]. So, gate length of 32nm is nearly an optimal value.

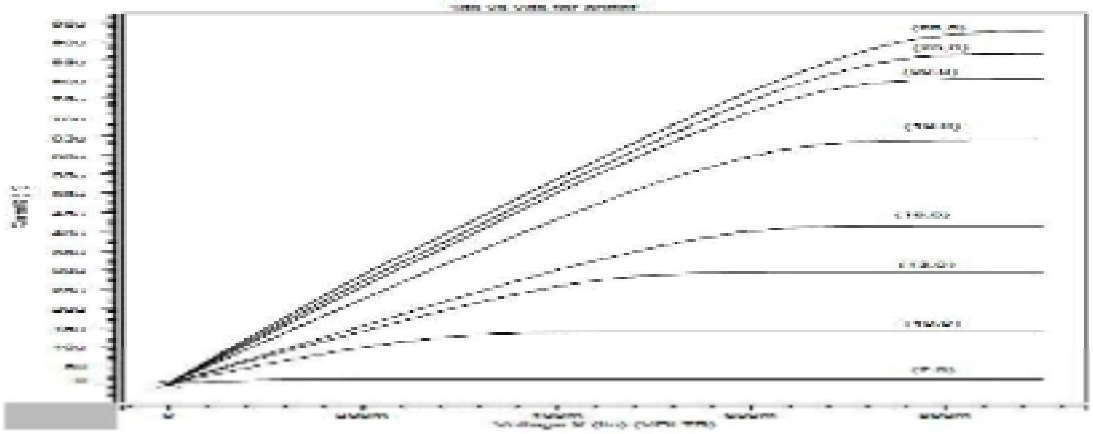

Fig. 7: Is depicted for Vg=0.9 in various chirality's (Marulanda and Srivastava, 2007).
The following relation exists between diameter and chirality:

$$D_{CNT} = \frac{\sqrt{m^2 + mn + n^2}}{\pi}$$

On the other hand, threshold voltage has a reverse relation with diameter which is clearly obvious in Fig. 7. As it could be seen in this figure, by increasing m in (m,n) pari, in fact, the diameter has increased and subsequently threshold voltage decreases. Thus, in lower voltages of gate we will have higher current.

3. DET flip flop

Many models have recently been developed by researchers in the field of double edge triggered flip flops (Lu and Ercegovac, 1990; Sung and Chang, 2004). Fig. 8 shows a pulse generator circuit and shows a flip flop circuit (Johnson and Kourtev, 2001) which are discussed below. The simplest way to trigger on both edges of clock signal is to use two latches, one on the rising edge and the other on the falling edge. Pulse generator is used as a logical XOR to trigger an impulse generator which is shown in fig (8) (Sung and Chang, 2004). When the clock signal A=CLK is increasing, for a short period of time, curve B is still high and curve C is still low. Then, M1, M3 and M4 turn off. Curve G will also discharge through M2 and goes down. By assuming that each Q1 to Q4 reversers produce a delay equivalent to τi, then Z = clk and Y = clk signals, through clock signal of A, take the values of $3\tau i$ and $4\tau i$, respectively. As such, after a delay of $4\tau i$, curve C will rise and curve G will charge and reach its maximum value. Similarly, when the clock signal A=CLK decreases, for a short period of time, curve B is still low and curve C is still high. Then, M2 turns off (Chang and Sachdev, 2008). Curve G discharges through M1, M3 and M4 and goes down. After a delay of $3\tau i$, curve B goes up and M1 and M3 turn on and turn off respectively. After a delay of $4\tau i$, curve C goes down and M4 turns off. Then, curve G discharges through M1 and goes up. G output signal will be equivalent to XOR of A and B signals.

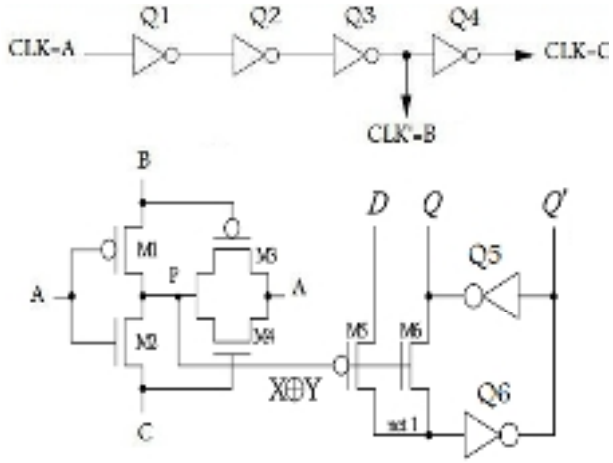

Fig. 8: Pulse generator circuit and DEF flip flop

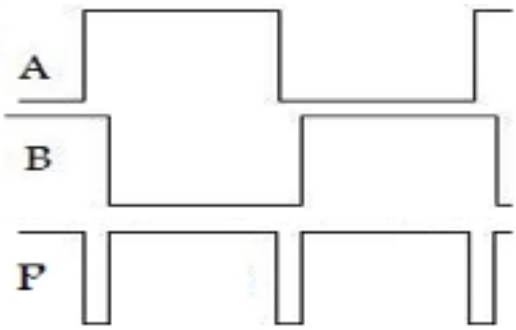

Fig. 9: Output of clock signal circuit (Lu and Ercegovac, 1990)

Fig. 9 shows the output of pulse generator circuit. After each clock signal that curve p goes down, there is a short period of time. During this short period of time, XOR output will get zero and subsequently M5 and M6 will turn on and turn off respectively. Then, D signal transfers the output to Q. Q5 and Q6 reversers keep the data and most of the input signals. D does not affect Q output (Mahmoodi-Meimand and Roy, 2008).

4. Suggested flip flop with CMOS and CNTFET transistors

In the following the design procedure of a triggered flip flop circuit with clock pulse edge is presented. In addition to reducing the power consumption in this design, reduction of leakage current and its associated power component are also considered. Fig. 10 shows the suggested low voltage double edge triggered flip flop circuit in a block form. This flip flop consists of two parts: a pulse generator and dynamic latches that are explained below.

Pulse generator is used as a logical XOR to trigger an impulse generator shown in Fig. 11. When the clock signal CLK is in a high state and out curve is still low and NAND gate output is in a high state and when NAND output falls down .In fact, the output of pulse generator takes an impulse form which is equivalent to XOR of both clk and out curves. Fig. 11 shows the suggested latch circuit. Latch only activates in the time interval of narrow pulses when its output nodes are initiated with respect to input values. When the signal is in a low state, MN1 and MN2 transistors are off and in this condition, latch circuit frequency is zero which means deletion of its dynamic power components. In this case, since MN1 and MN2 transistors are off, there is no need for cutoff transistors and leakage current will reduce in paths leading to it. Nevertheless, in this condition, there is some leakage current in other parts of the circuits and in the latch part (MP1, MP2, MN3, MN4) which should be reduced using appropriate methods while keeping the circuit speed. Fig. 12 shows the same structure using CNTFET transistors.

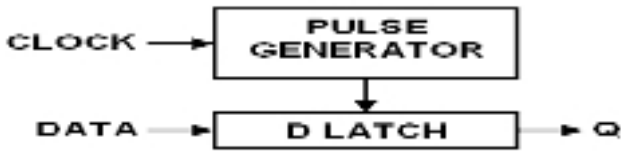

Fig. 10: Block diagram of suggested flip flop

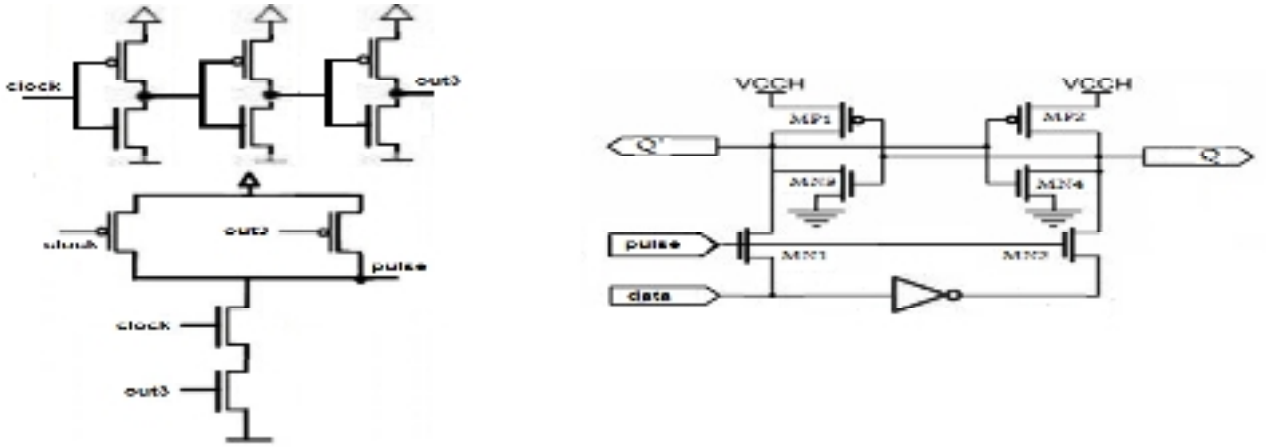

Fig. 11: Suggested impulse generator and flip flop-latchcircuit with CMOS transistor

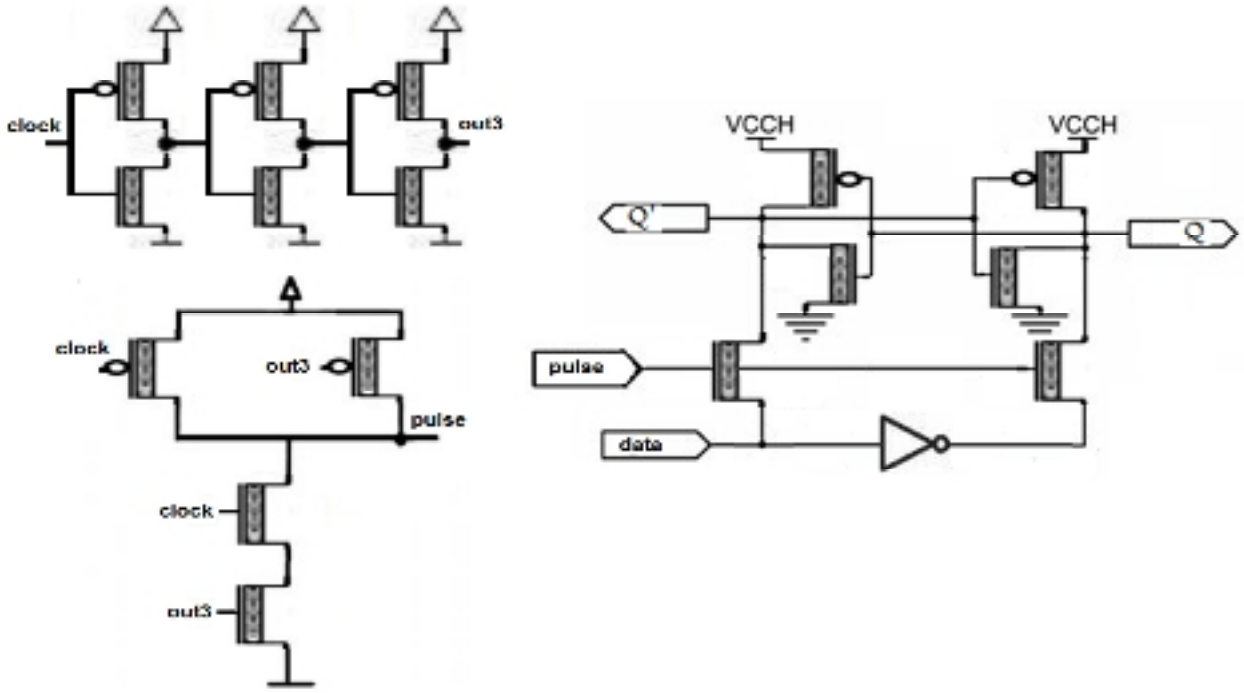

Fig. 12: Suggested impulse generator and flip flop-latch circuit with CNTFET transistor

5. Simulation results

The results were obtained through simulation using HSPICE software and 0.32 technologies in MOS model of MOSIS for CMOS transistors [17]. Furthermore, the value of aspect ratio for all transistors in the normal state was equivalent to 0.32/0.32. Also, all the obtained results are available. The model developed by Stanford University was used to simulate CNTFET transistors [20]. The suggested flip flop circuit operated by a supply voltage of VCC=1 V. Fig (13) shows the simulation results which are the same for both CMOS and CNTFET. Waveforma is the reference clock pulse and waveform b is the narrow pulses generated in both edges of clock pulse. Waveform c is the input data and waveform d shows the functionality of flip flop. When there is data, output also follows the input data and retains its previous state until input data changes. Maintaining accurate information occurs along with reduction of leakage current. Waveforme is the complement of input data. Figs (13-15) show this value for CMOS and CNTFET transistors,

respectively. As it is clearly obvious, in higher frequencies, CMOS transistors do not appropriately follow the input but CNTFET transistor show a good compliance and high performance.

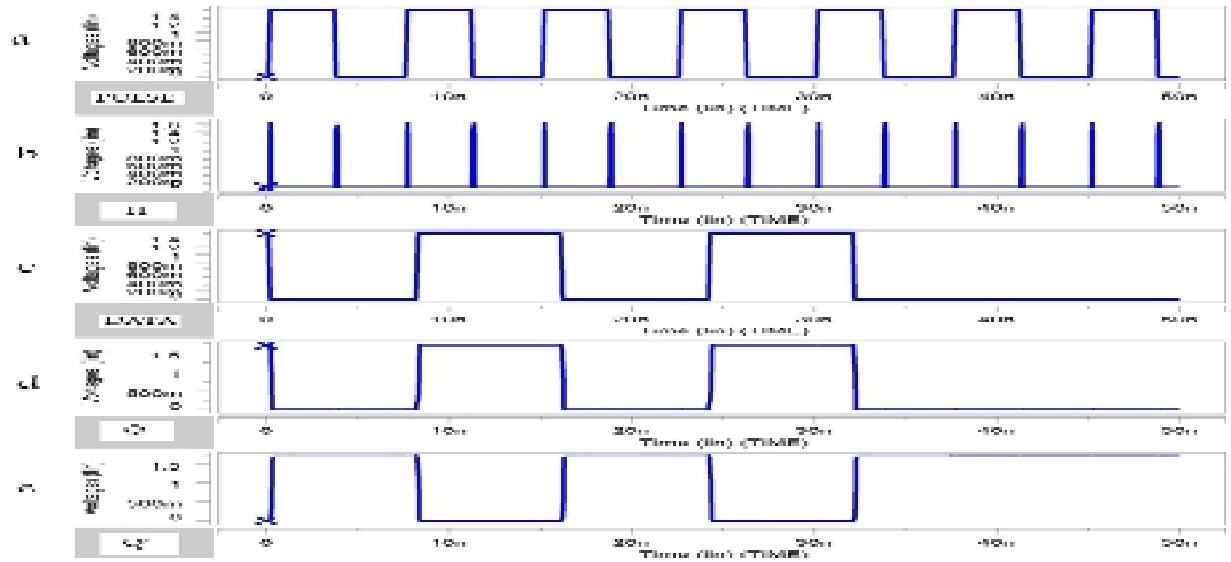

Fig. 13: Simulation results, (a) clock pulse, (b) , impulse, (c) input data, (d) flip flop output, (e) output complement of flip flop for both CMOS and CNTFET

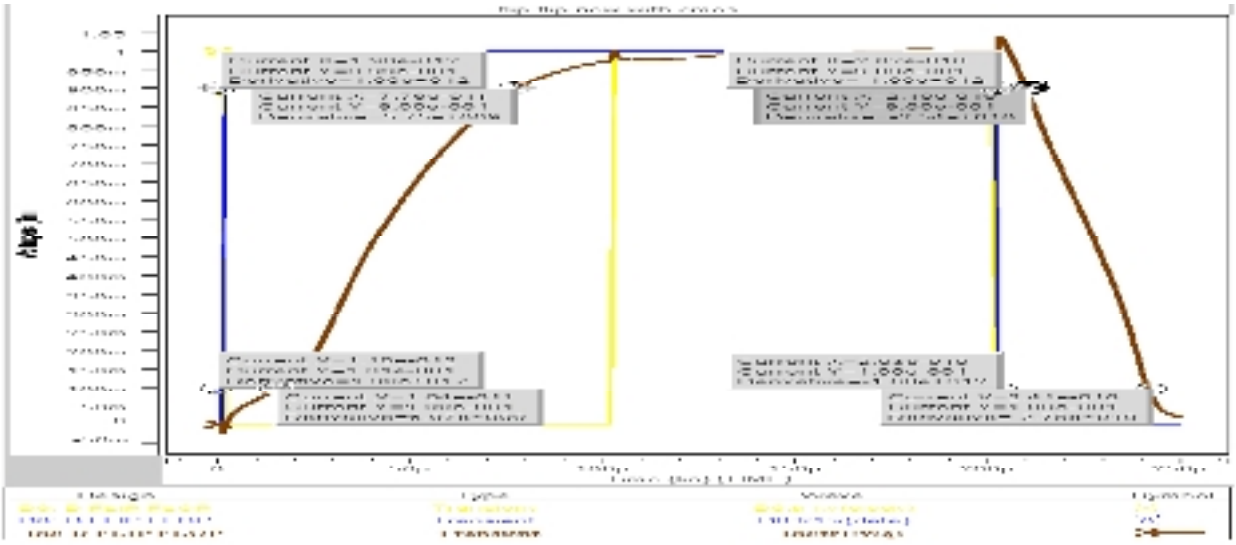

Fig. 14: Suggested circuit output using CMOS transistors

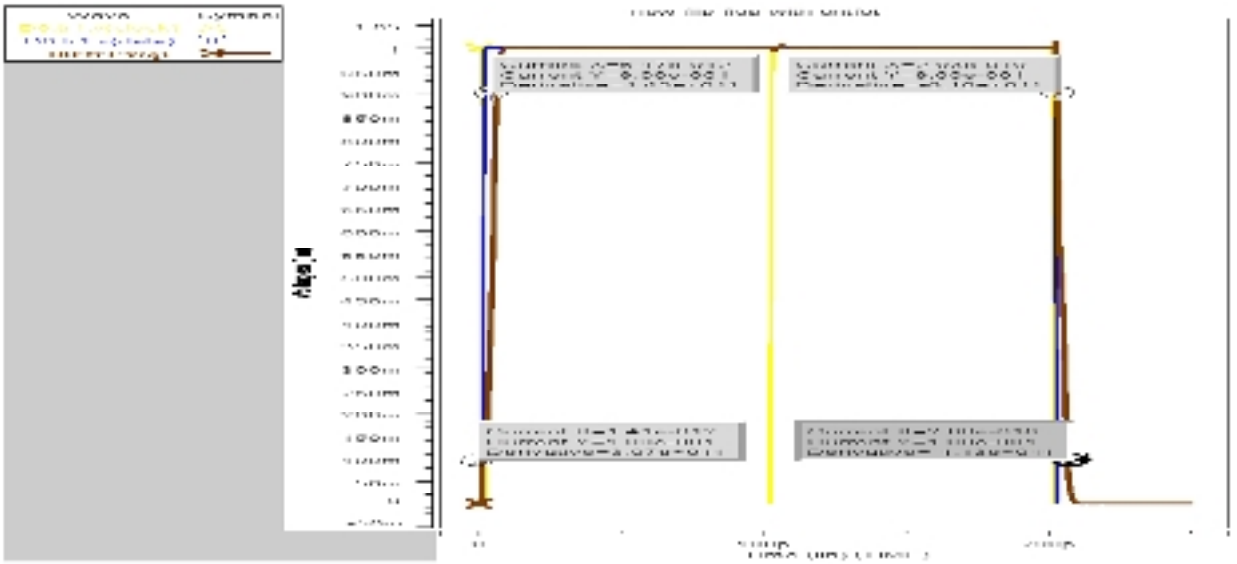

Fig. 15: Suggested circuit output using CNTFET transistors

Table 1: Comparison between MOSFET and CNTFET flip flop

Flip flop	Number of transistors	Rise time Q (s)	Fall time Q (s)	Delay fall time (s)	Delay rise time (s)	Power (w)	PDP	Voltage supply	swing
Suggested flip flop with CMOS	18	61.2p	31ps	24p	39.5p	1.577n	39.5p*1.577n= 62.3e-21	1v	1v
Suggested flip flop with CNFET	18	4.76p	0.03ps	2p	3.18p	0.8744n	3.1p*0.8744n= 2.71e-21	1v	1v
Reference flip flop	18	400n	280ns	405n	410n	47.8u	410n*47.8u=19.6fj	1.5v	1v
Percent improvement in technology	0%	92.32%	99%	91.66%	91.91%	44.55%	95.65%	0%	0h

6. Conclusion

In the present study, CNTFET carbon Nanotube transistors were studied and then two types of CMOS and CNTFET transistors were compared and eventually a new flip flop with low power consumption and leakage current was introduced to be used in the design of low power-high speed digital circuits. The structure of the circuit is such that beside low leakage current, it has a high speed. In this work, low power consumption was obtained due to the new suggested flip flop structure and using CNTFET transistors. According to the results, CNTFET can be a good substitute for CMOS transistors since it has higher speed and lower power consumption. Results indicate the good functionality of suggested flip flop.

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