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Modeling and evaluation of optimal T-flip flap based on quantum Cellular Automata using QCA designer simulator

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Abstract: Quantum Cellular Automata (QCA) offers a new approach to building computer circuits. Since memory is one of the most applicable basic units in digital circuits, but Its smaller components, which are called by flip-flop is created. Although there are some QCA structures for a memory cell in the literature, however, QCA characteristics may be used in designing a more optimized memory cell than blindly modeling CMOS logics in QCA. It is trying to propose a new design of the T-ff be paid within QCA. It is designed to lower the number of cells used to build T-ff. Simulation of the proposed structure is performed by means of QCA Designer Simulator and is compared with common structure from the view point of number of cells, area, and speed.

Key words: Quantum Cellular Automata; T – flip flap; Simulator

1. Introduction

Fundamental physical limitation of CMOS technologies, make extensive research in recent years in nanotechnology for future generation IC. Gordon Moore has predicted, in 1965, that the capacity of a computer chip would grow exponentially with time. Since then, the so-called Moore's Law had governed the development and performance of microprocessors. Shrinking transistors has been the major trend to achieve circuits with fast speed, high densities and low power dissipation. However, when scaling comes down to submicron level, many problems occur. Physical limits such as high power consumption and design complexity may hold back the further progress of microprocessor performance, other technologies should be studied.

As an attractive alternative CMOS-VLSI, researchers have proposed an approach to computing with quantum dots, the quantum cellular automata (QCA). It was proposed by Lent et al. in 1993. QCA is based upon the encoding of binary information in the charge configuration within quantum dot cells. Computational power is provided by the Columbic interaction between QCA cells. No current flows between cells and no power or information is delivered to individual internal cells. The local interconnections between cells are provided by the physics of cell-to-cell interaction due to the rearrangement of electron positions. Recent papers show that QCA can achieve high density, fast switching speed, and room temperature operation (Askari et al, 2011).

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2. Quantum-Dot Cellular Automata (QCA)

Quantum-dot is a Nano-technology structure made up of semiconductors, such as GaAs, InAs. As shown in Fig. 1, each cell contains four quantum dot in which electrons have been trapped and do not have enough energy to run away. This structure is likely to be produced in quantum-scaled square patterns.

In 1993, the concept of QCA was introduced based on the effectiveness of the adjacent cells. This is the concept of a Von Neumann computational machine that works based on the polarization of majority of the neighboring cells. As shown in Fig. 1, a quantum cell consists of four quantum dots and is capable of enjoying two stable arrangements. These two arrangements have been denoted as cell polarization p=+1 and p=-1, respectively. The bipolar cell p=+1 represents logic "1", and p=-1 represents logic "0" (Dehkordi et al, 2011).

Generally, an unvalued cell changes into 1 only if the number of its adjacent 1 s is greater than the number of its adjacent 0 s.

There are many activities regarding the performance of primary structure, such as one-bit adder[Wang and et al,2003,461-464], a variety of adders (Zhang et al, 2005), binary multipliers (Hanninen et al, 2007), barrel shifters (Vetteth et al, 2002), field-programmable gate arrays (Timothy et al, 2006), investigation of fault tolerance in some of the structure (Xiaojun et al, 2008), RAM cells (Walus et al, 2003), and QCA memory architecture (Vankamamidi et al, 2008).

In QCA, there are two general structures, line-based and loop-based, for a RAM cell. In a line-based RAM cell, storage is accomplished through a QCA line

as the basic configuration for a memory cell. In this type of memory cells, data are moved back and forth along a line as stated in Baris et al (2008). Line-based RAM cells require additional clock zone which make their implementation complex. However, in loop-based RAM cells, storage mechanism is done by circulating a bit in a closed QCA loop, which consists of all the four clocking zones to be elaborated on. As the implementation of a loop-based RAM cell makes use of no additional clock zones, they are preferred more and this paper focuses on this type of RAM cells. However, common Loop-based RAM cells such as are not optimized enough and have not considered regularity of clock zones in their design in contrast to line-based methods. Also the length of the longest lines increases their sensitivity to thermal fluctuations. These shortcomings make their realization troublesome.

2.1. Fundamental logics in QCA

In this section, the general logics and gates in QCA are investigated in the order of wires, inverters, majority gates, AND, and OR gates.

2.1.1. QCA wire

As shown Fig. 2, the adjacent cells employ the same polarizations; if the polarization; if the polarization one of cell changes, it enforces its adjacent cells to change due to electron repulsion. Thus, the binary input value applied to one end of a QCA wire will be propagated to the other end.

Fig. 3 illustrates another case of QCA wire where its cells are oriented at 45^. In this wire case, the polarization of each cell will be opposite of its adjacent; this feature can be used in inversion.

2.1.2. Inverter gate

An inverter gate is shown in Fig. 4 where a Columbic repulsion between the corners of the parallel cells makes the polarization of the starred cell to change into the opposite polarity of the input.

2.1.3. Majority, AND, and OR gates

The majority gate (majority voter) that is shown in Fig. 5, is the elementary gate in designing QCA based circuits. The majority gate acts as a three input logic function. Assuming that the inputs are A, B and C, the logic function of the majority gate is shown as M(A,B,C)=AB+AC+BC

If one of the input cells in the majority gate is constantly fixed to +1, one of the other cells is required to be +1, so that the polarity in output cell is +1. In fact, it behaves like an OR gate and is represented as

M(A,B,1)=AB+(A1)+(B1)=AB+A+B=A+B

By fixing the polarization of one input cell to -1, it is clear that the other two inputs must be in +1 polarization to result in +1 polarization in the output cell. In fact, this structure acts like an AND gate and is demonstrated as

M(A,B,0)=AB+(A0)+(B0)=AB

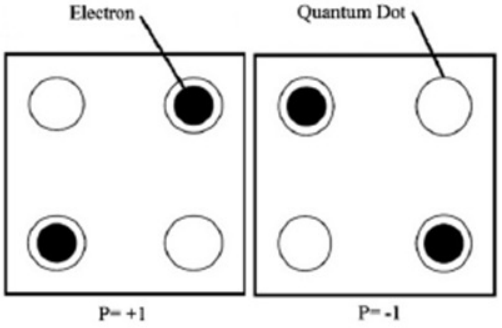

Fig. 1: Basic QCA cell and binary encoding

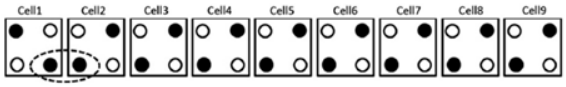

Fig. 2: QCA wire structure

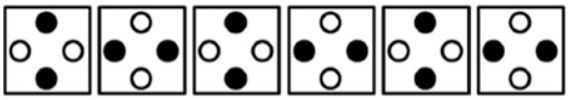

Fig. 3: Inverter chain

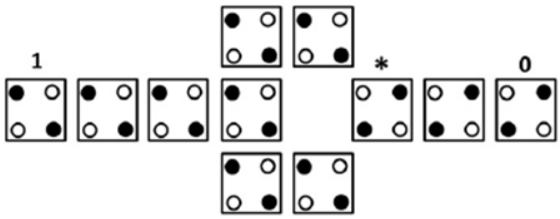

Fig. 4: QCA inverter gate

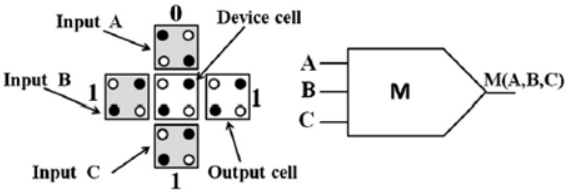

Fig. 5: Majority gate structure

QCA circuits need to a clock signal for synchronization of information and control them. This technology, requires to clock not only to sequential circuits but the clock signal is the requirement for operate both of sequential and combinational logic, because clock signal provides power to run the circuit. For QCA circuits, the clock signal through the electric field is produced, that is applied to cells until to take up or down the tunneling barrier between quantum-dots within a cell (Frost, 2002). When the potential barrier is low, the cell is un-polarized, and when the potential barrier is high, cells cannot change their state. In QCA clock signal includes four phases: switch phase, hold phase, release phase, relax phase, respectively as shown in Fig. 6. Surface of circuit is divided into parts; each area is called a clock zone. To each of the

clock zone, one of the phases will be allocated as shown in Fig. 6. Each of the clock zones has a 90 degrees phase difference with next clock zone. During the first clock phase, namely switch phase, quantum cells being unpolarized. The potential barriers gradually rose during this clock phase and the quantum cells are polarized by influence of their driver cell. During the second phase, namely hold clock phase, the potential barriers are fixed high and cells that located in hold phase can be use as driver cell to next ster. In the next clock phases namely release clock phase, potential barriers become low and cells are unpolarize. In final clock phase, namely relax clock phase, potential barriers remain low and quantum cells are unpolarize.

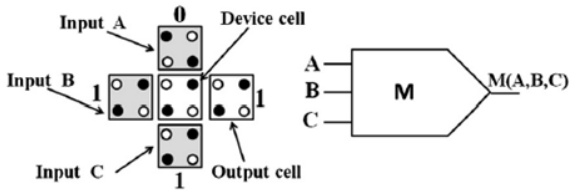

Fig. 6: Four phases of QCA clock signal. (b) Clocking zones

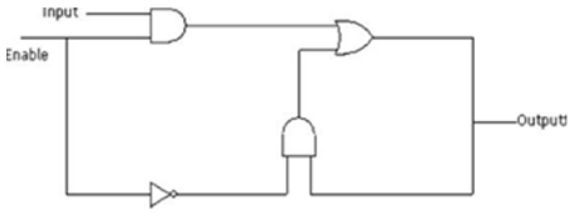

Fig. 7: T flip-flop. circuit diagram

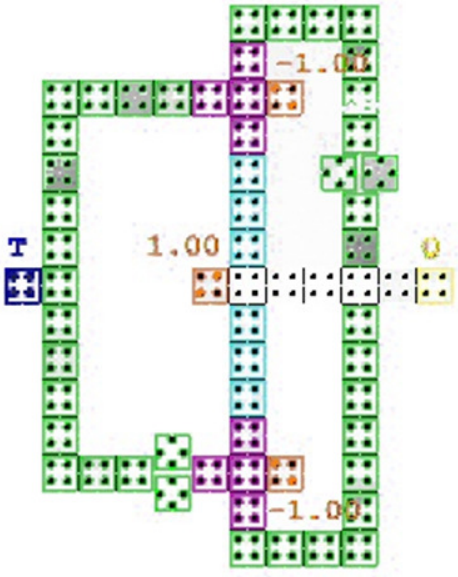

Fig. 8: QCA layout of T flip-flop

2.2. Common Structure of TFF

The common model for T flip flap is made from basic gates such as OR, AND, NOT. General design for TFF is shown in figure 7.

Construction of this structure based on QCA is indicated in figure 8. in this structure 63 cells are used for making TFF.

Fig. 8. QCA layout of T flip-flop..

The results of simulation regarding the common structure are shown in figure 9. the output of the simulator shows that four regions of clock are used to produce the correct output.

Fig. 9. Simulation results of T flip-flop

3. The improved approach

In the method mentioned in former section for construction of TFF, we utilized 63 cells, 4 regions of clock to produce the appropriate output. Since parameters such as large area, and long wires are from the main obstacles (Walus, 2003) in this paper a new approach with fewer cells and smaller area is proposed for construction of TFF. This approach which is based on QCA is indicated in figure 10. In this structure we used 47 cells to produce TFF. The result of this simulation is shown in figure 11.In this proposed design we used 47 cells which is improved about 25% comparing with the previous design. Meanwhile, the occupied area is 25% less than former design. Transition of the input to the output is performed in 4 regions of the clock, as it was in the former approach.

4. Conclusion

As it was mentioned, designation of circuits based on QCA is considered to be of great interest, because of its good properties. In this technology, factors such as number of cells and length of the root is effective in evaluation of output quality, reduction of complexity, dimensions of the circuit, and finally, speed.

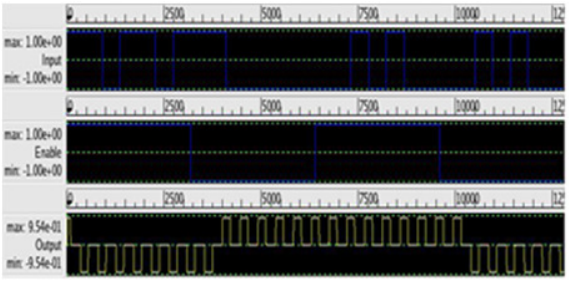

Fig. 9: Simulation results of T flip-flop

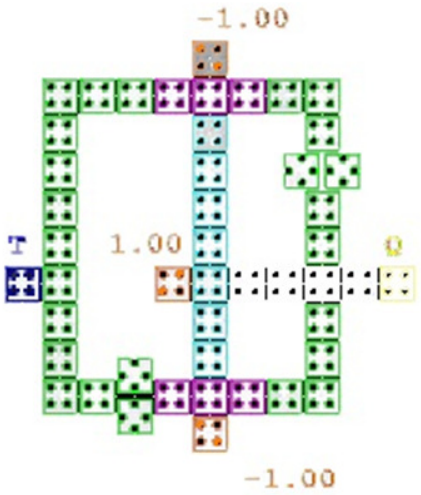

Fig. 10: QCA layout of a T flip-flop

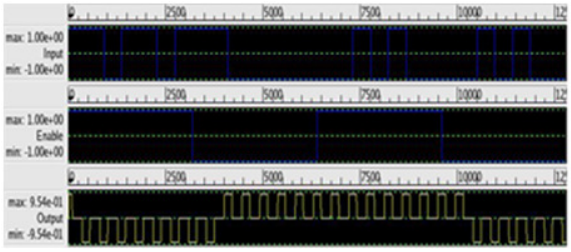

Fig. 11: result of simulation QCA Designer T flip-flop

In this paper a new structure was proposed for TFF which utilizes fewer cells comparing with common structure, meanwhile transition speed of input to output has not changed in comparison with former approach.

References

A. Vetteth, K. Walus, V. Dimitrov, G. Jullien, Quantum-dot cellular automata carry-look-ahead adder and barrel shifter, in: Proceedings of the IEEE Conference on Emerging Telecommunications Technologies, Dallas, TX, September 23–24, 2002.

A.S. Shamsabadi, B.S. Ghahfarokhi, K. Zamanifar, N. Movahedinia, Applyinginherent capabilities of quantum-dot cellular automata to design: D flip-flopcase study, Journal of Systems Architecture 55 (2009) 180–187.

Askari, M., M. Taghizadeh, 2011. Logic Circuit Design in Nano-Scale using Quantum-Dot Cellular Automata, in Proc. European Journal of Scientific Research, pp: 516-526, ISSN 1450-216X Vol.48 No.3 (2011).

B.K. Mathew, S.K. John, C. Pradeep, New technique for fault detection inquantum cellular automata, IEEE Proceedings (2008).

Baris Taskin, Bo Hong, Improving line-based QCA memory cell design through dual phase clocking, IEEE Transactions on VLSI 16 (12) (2008) 1648–1656.

I. Hanninen, J Takala, Binary multipliers on quantum-dot cellular automata, Facta Universitatis (NIS) Series: Electronics and Energetics 20 (3) (2007) 541–560.

K. Walus, A. Vetteth, G.A. Jullien, V.S. Dimitrov, RAM design using quantumdotcellular automata, in: Technical Proceedings of the NanotechnologyConference and Trade Show, vol. 2, 2003, pp. 160–163.

M. A. Dehkordi, A. S. Shahini, B. Shahgholi Ghahfarokhi, A. Vafaei, Novel RAM Cell Designs based on Inherent Capabilities of Quantum-Dot Cellular Automata, Microelectronics Journal 42 (5), 2011.

M. Ottavi, S. Pontarelli, V. Vankamamidi, F. Lombardi, Novel memory designs for QCA implementation, in: Proceedings of the IEEE NanotechnologyConference, Paper WE P7-4, IEEE Number: 05TH8816C, ISBN: 0-7803- 9200-0, Nagoya, Japan, July 2005.

R. Zhang, K. Walus, W. Wang, G. Jullien, Performance comparison of quantum-dot cellular automata adders, in: Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Kobe, Japan, May 23–26, 2005, pp. 2522–2526

S. Frost, A. Rodrigues, A. Janiszewski, R. Rausch, P. Kogge, Memory in motion: a study of storage structures in qca, in: Proceedings of the First Workshop on Non-Silicon Computing, 2002

Timothy Lantz, Eric Peskin, A QCA implementation of a configurable logic block for an FPGA, in: Proceedings of the IEEE International Conference on Reconfigurable Computing and FPGA's, San Luis Potosi, September 2006, pp. 1–10.

Vamsi Vankamamidi, Marco Ottavi, Fabrizio Lombardi, A serial memory by quantum-dot cellular automata (QCA), IEEE Transactions on Computers 57 (5) (2008).

W. Wang, K. Walus, G. Jullien, Quantum-dot cellular automata adders, in: Proceedings of the IEEE Conference on Nanotechnology (NANO), San Francisco, CA, August 11–14, 2003, pp. 461–464.

W.J. Townsend, J.A. Abraham, Complex gate implementations for quantum dot cellular automata, in: Proceedings of the Fourth Conference on Nanotechnology, 2004, pp. 625–627.

Xiaojun Ma, Fabrizio Lombardi, Fault tolerant schemes for QCA systems, in:Proceedings of the IEEE International Symposium on Defect and FaultTolerance of VLSI Systems, 2008.