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Design and noise optimization of inductive source degeneration LNA using PSO technique

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Abstract: This paper details an optimized design of a low noise amplifier by employing a swarm intelligence based technique called Particle Swarm Optimization (PSO). To reduce the noise figure, a cascade structure with inductive source degeneration LNA is proposed and it is validated through CADENCE simulations in standard 0.18µm process. This LNA also increases the gain and save power consumption. It exhibits minimum noise figure of 1.55 dB, gain of 19.8dB and input return loss of -35 dB respectively.

Key words: Low noise amplifier; Particle swarm optimization; Inductive source degeneration; Heuristic optimization; Classical optimization

1. Introduction

Due to its tendency to dominate the sensitivity, low noise amplifier (LNA) has become one of the main components in a typical RF receiver (Razavi, 1997).But for a given technology its sensitivity has direct impact on the LNA components i.e. both on active and passive components. Therefore, the chosen technology will be responsible for the final achievable targets. Because of technology scaling, low cost and higher degree of integration, CMOS has become one of the most demanding technologies for radio transceiver implementation (T. H. Lee, 2002). Hence we must be able to design a CMOS LNA with very low noise. Apart from low noise, it should have high linearity, high gain and low power consumption. Different topologies are provided for designing LNA such as resistive termination common source, common Gate, shunt series feedback common source, inductive degeneration common source and cascode inductor source degeneration. In order to design a low noise LNA, the best option is to adopt a cascade structure with an inductive source degeneration configuration (Shaeffer, 1997) which is shown in Fig. 1. This topology provides good in-out isolation and is the most practicable topology.

In LNA design one of the most important parameters is optimizing the noise Fig.ure (NF) but optimization of an analog circuit is a very time taking process. Another demerit of analog synthesis is its complication due to its various topologies, layout synthesis and component sizing (Graeb, 2001). To overcome these problems, an automated design and optimization techniques are used. And one of such optimization technique is Particle Swarm Optimization (PSO) that was developed by Kennedy and Eberhart in 1995 (Kennedy J, 1995). Among the other optimization techniques, PSO is best suited for analog circuit and optimization such as automatic sizing of low power analog circuit (David J, 2004).

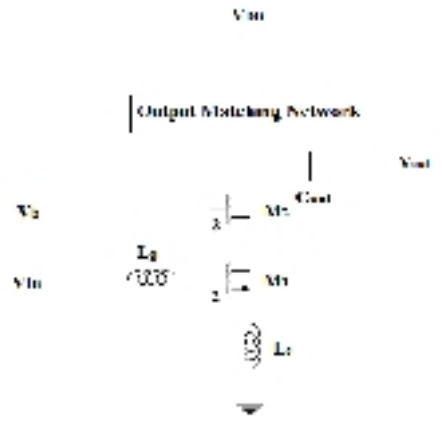

Fig. 1: Cascode Inductive Source Degeneration Topology

Therefore in this paper PSO technique is employed for automated design and optimization on the inductive source degeneration LNA.

2. LNA design and its analysis

2.1. Description of LNA design

In receiver design a cascade is designed usually with inductive source degeneration topology because it provide best matching for both noise Fig.ure and power gain. A common-source structure is combined with a common-gate to form the cascade structure whose main purpose is to increase gain of the LNA and the output impedance while protecting from unpleasant experience (Scholten, 2003).

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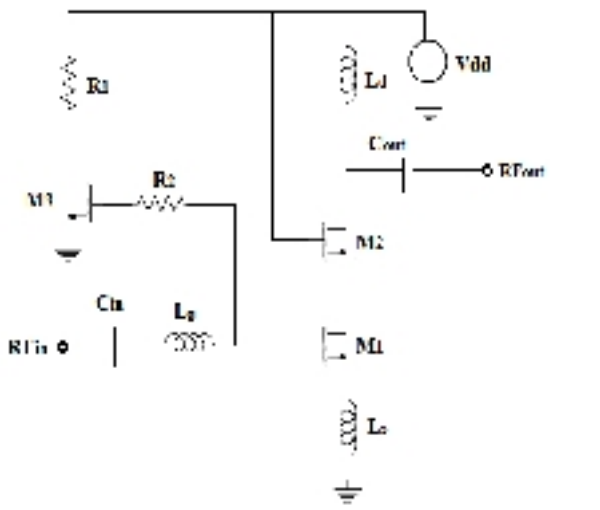

Fig. 2: Cascode LNA with Inductive Source Degeneration Topology

Fig. 2 shows the complete schematic LNA where M_1 and M_2 are same size RF transistor which provide good noise isolation. In the noise analysis of LNA, transistor M_1 is referred because M_2 has minor influence on the total noise of the LNA. M_2 is cascading transistor which is used to reduce the effect of the gate-drain capacitance of M_1. The values of source inductor L_s and gate inductor L_g are chosen in such a way that it can provide the desired input resistance. M_3 is the current mirror transistor of M_1 and $M_3 R_1 R_2$ form the bias circuit. L_d and capacitance of M_2 form the tank circuit which will provide a DC path for the bias current for both M_1 and M_2

2.2. Noise analysis

In a MOS transistor noise is mainly dominated by the intrinsic part of the active device (A van der Ziel). For radio frequency (RF), the total noise is defined by the thermal noise component. Noise behavior of the LNA is majorly due to M_1 of Fig. 2 whereas M_2 has minor contribution to the total noise.

Thermal noise of the source resistance (i_{nR_s}), thermal noise of the channel current (i_{nd}), and the gate induced current noise (i_{ng}) and the thermal noise of the output resistance (i_{nRout}) are the main source of noise of LNA. Therefore the noise densities are given as

$$\overline{i_{n,R_s}^2} = 4kT\frac{1}{R_s}\Delta f \quad (1)$$

$$\overline{i_{n,R_{out}}^2} = 4kT\frac{1}{R_{out}}\Delta f \quad (2)$$

$$\overline{i_{n,d}^2} = 4kT\gamma g_m \Delta f \quad (3$$

$$\overline{i_{n,g}^2} = 4kT\beta\frac{(\omega C_{gs})^2}{g_{dn}}\Delta f \quad (4)$$

Where $g_{dn} = \frac{2}{3}g_{do} = \gamma g_{do} = \gamma g_m$ from (K. K. Hung, 1990). Here g_{dn} depend on the transistor adopted. But at saturation g_{do} is equal to g_m. β can be adjusted for increase of $\overline{i_{n,g}}$ due to short channel effects.

The values of γ and β for long channel devices are respectively

$$\gamma = 1 \quad (5)$$

$$\beta = 8/45 \quad (6)$$

The transistor operating in saturation has drain current I_{ds} of

$$I_{ds} = \frac{1}{2}\mu_{eff}C_{ox}\frac{W}{L}V_{od}V_{dsat} \quad (7)$$

Where $\mu_{eff} \approx \frac{\mu_n}{1+\theta V_{od}}$ (8)

$$V_{dsat} \approx \frac{V_{od}V_{sat}}{V_{od}+A_bV_{sat}} \quad (9)$$

$$V_{sat} \equiv E_{sat}L = 2\frac{v_{sat}}{\mu_{eff}}L \quad (10)$$

By definition g_m is given as

$$g_m = \frac{\partial I_{ds}}{\partial V_{od}} \quad (11)$$

Therefore using equation (11) we can write the expression for g_{dn} as

$$g_{dn} = \mu_{eff}C_{ox}\frac{W}{L}\left[V_{od}\frac{A_bV_{dsat}}{2}+\frac{(A_bV_{dsat})^2}{6(2V_{od}-A_bV_{dsat})}\right] \quad (12)$$

Equation (12) defines the effects of charge carrier velocity saturation on noise. And from equation (4) and (12), it can be state that $\overline{i_{n,g}^2}$ increases with increasing V_{od}. Now let's consider a case in which V_{sat} is much larger than V_{od}. Here for simplicity we will take μ_{eff} as constant and under such condition, g_m and g_{dn} becomes (T. Manku, 1999)

$$g_m = \sqrt{\frac{2}{A_b}\mu_{eff}C_{ox}\frac{W}{L}I_{ds}} \quad (13)$$

$$g_{dn} = \gamma\mu_{eff}C_{ox}\frac{W}{L}V_{od} \quad (14)$$

$$\frac{g_{dn}}{g_m} = \gamma A_b \quad (15)$$

We can further simplify the expression by assuming as

$$\gamma' = \gamma A_b \quad (16)$$

$$\beta' = \beta/A_b \quad (17)$$

$$\mu_{eff}' = \mu_{eff}/A_b \quad (18)$$

Using the above equations we can write the expression for noise Fig.ure as

$$F = 1+\frac{\beta'\left(Q^2+\frac{1}{2}\right)\left(Q\frac{4}{3}\omega_o R_s C_{ox}WL\right)^2+\gamma'/4}{R_s Q^2\sqrt{2\mu_{eff}'C_{ox}WI_{ds}/L}} \quad (19)$$

Where ω_0 is resonance angular frequency and Q is the quality factor of the input circuit which is equal to

$$\omega_0 = \frac{1}{\sqrt{L_t C_t}} \quad (20)$$

$$Q = \frac{1}{2R_s\omega_0 C_t} \quad (21)$$

Here $L_t = L_g + L_s$ (22)

$$C_t = C_d + C_{gs} \quad (23)$$

Applying equations (20) and (21) in (19) we get

$$F = 1 + xQ^2 W^{3/2} + \frac{x}{4}W^{3/2} + yQ^{-2}W^{-1/2} \quad (24)$$

Where expression for x and y can be easily perceived. Generally Q are limited for certain reasons such as sensitivity and linearity and also for a given I_{ds} there should be large W. Therefore fixing the value of Q and taking the derivative of equation (24) w.r.t W will give

$$\frac{\partial F}{\partial W} = \frac{3}{2}x\left(Q^2 + \frac{1}{4}\right)W^{1/2} - \frac{1}{2}yQ^{-2}W^{-3/2} \quad (25)$$

Optimal transistor width W_{opt} can be defined by equating equation (25) equal to zero. After simplifying the final expression, W_{opt} is obtained as

$$W_{opt} = \frac{A_b}{2Q^2}\sqrt{\frac{5}{6}}\frac{1}{4/3\omega_0 R_s C_{ox} L} \quad (26)$$

Therefore for a given Q, minimum noise Fig.ure is given as

$$F_{\min} = 1 + \frac{\left(Q^2 + 1/4\right)^{1/2}}{Q^{3/2}} 4x^{1/4}\left(\frac{y}{3}\right)^{3/4} \quad (27)$$

$$\approx 1 + \frac{1}{Q}4x^{1/4}\left(\frac{y}{3}\right)^{3/4} \quad (28)$$

$$F_{\min} = 1 + \frac{1}{Q}4\beta'^{1/4}\left(\frac{\gamma'}{12}\right)^{3/4}\sqrt{\frac{2\omega_0}{3\mu_{eff}' R_s I_{ds}}}L \quad (29)$$

2.3. Particle swarm optimization

In order to design a high performances circuits the main target is to optimize the size of the analog components (Toumazou, 1993) and this optimization method involve solving of various variables, objectives and constraints function simultaneously. Due to this complexity the Classical Optimization technique is not a good option. One optimization technique that is well suited for such type of approach is nature inspired heuristic optimization algorithm called Particle Swarm Optimization (PSO) which centered on the intelligence of swarm (Clerc, 2006). A comparison of Classical and Heuristic optimization technique is shown in Fig. 3.

For any analog circuit, we deal with the general analog constraint optimization problem whose format is defined as

Minimize $f(\vec{x});\ f(\vec{x}) \in R$ (30)

Such that $\vec{g}(\vec{x}) \le 0;\ \vec{g}(\vec{x}) \in R^m$ (31)

$$\vec{h}(\vec{x}) = 0;\ \vec{h}(\vec{x}) \in R^n \quad (32)$$

Where $x_{Li} \le x_i \le x_{Ui}$ and $i \in [1, p]$. Here f(x) represents the objective function, g(x) and h(x) represents m inequality and n equality constraint functions respectively. P parameters to manage $\vec{x}_L$ and $\vec{x}_U$ are vectors that will determine the lower and upper boundaries of the parameters.

But for a MOSFET amplifier there are multiple objective functions such as gain, noise Fig.ure, bandwidth etc. that is to be optimized. For this condition equation (30) need to be modify

Minimize $f(\vec{x});\ f(\vec{x}) \in R^k$ (33)

Subjected to $\vec{g}(\vec{x}) \le 0;\ \vec{g}(\vec{x}) \in R^m$ (34)

$$\vec{h}(\vec{x}) = 0;\ \vec{h}(\vec{x}) \in R^n \quad (35)$$

Here k is the number of objectives where $k \ge 2$. The purpose of optimization process is to minimize an objective function $f(\vec{x})$. Maximizing $f(\vec{x})$ can also be done by minimizing $-f(\vec{x})$.

Multiple candidate solution are considered in PSO algorithm where each candidate is called a particle which is associated with a randomized velocity (Chan, 2007). Also each particle mush remember its best position ($Pbest$) in the problem search space and ($Gbest$).

For example, let's consider a i^{th} particle in the N-dimensional search space where the i^{th} particle and its velocity, best position and global best position are represented as

$$X_i = \left(x_{i.1}, x_{i,2}, \ldots x_{i,N}\right) \quad (36)$$

$$V_i = \left(v_{i,1}, v_{i,2}, \ldots v_{i,N}\right) \quad (37)$$

$$(p_{best})\ p_i = \left(p_{i,1}, p_{i,2}, \ldots p_{i,N}\right) \quad (38)$$

$$g = \left(g_1, g_2, \ldots g_N\right) \quad (39)$$

This i^{th} particle update the values of velocity and position by using the equation given below (Chan, 2007)

$$V_i^{t+1} = \underbrace{wV_i^t}_{Inertia} + \underbrace{c_1 r_1\left(P_i^t - X_i^t\right)}_{\substack{Personal \\ influence}} + \underbrace{c_2 r_2\left(P_i^t - X_i^t\right)}_{\substack{Social \\ influence}} \quad (40)$$

$$X_i^{t+1} = X_i^t + V_i^{t+1} \quad (41)$$

Where diversification feature of the algorithm is controlled by an inertia weight, w. c_1 and c_2 control the particle attitude that searches its beat location. And each dimension are uniformly sampled in [0,1] by using two random values r_1 and r_2. Flowchart of a standard PSO is shown in Fig. 4

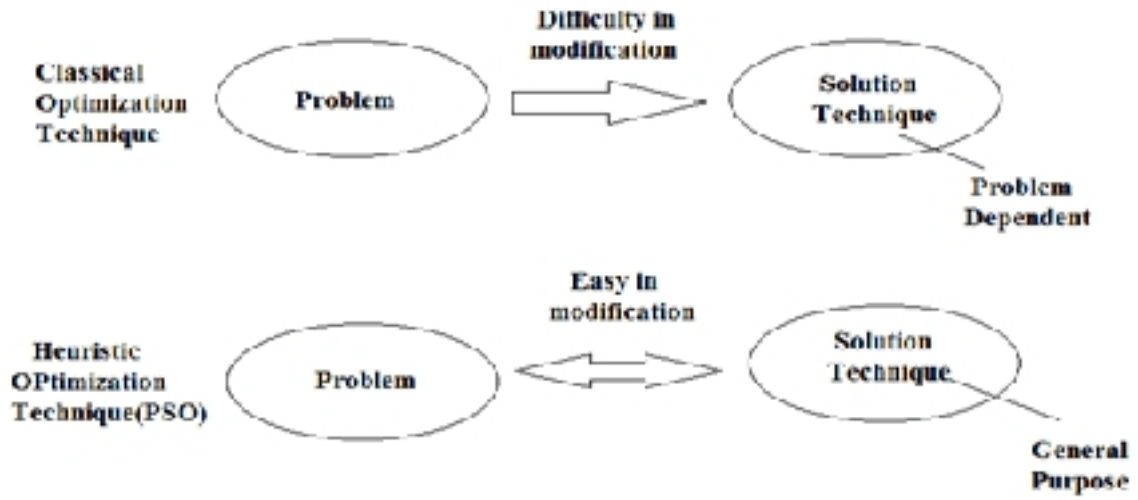

Fig. 3: Comparison of classical and modern heuristic optimization techniques

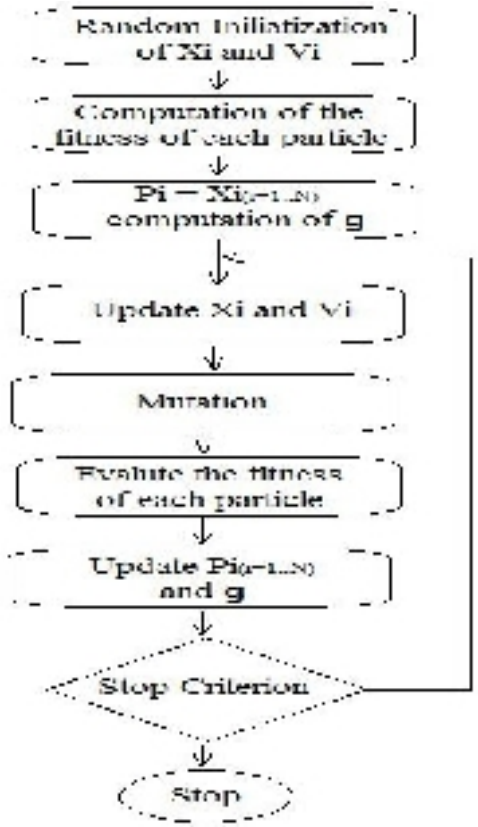

Fig.4: Flowchart of a standard PSO

In this paper optimization is done by using LNA noise figure as objective function whose expression is shown in equation (29). And the constraints for this LNA design are gain, stability, impedance and small circuit sizing.

3. Result

The proposed LNA design is implemented in UMC 0.18µm CMOS technology and by using PSO algorithm the optimum values of the circuit components are calculated. PSO algorithm parameters and its optimal parameter's values are given in table 1 and table 2 respectively.

Table1: Parameters of PSO algorithm

Size of the swarm	Number of iterations	C_1	C_2	ω
30	1000	1	1	0.4

Table 2: Optimal parameter's values

W_1/L_1 (µm)	W_2/L_2 (µm)	L_g	L_s	L_d	C_{in}	C_{out}
240/0.18	160/0.18	3.2 nH	450 pH	1.6 nH	630 pF	470 fF

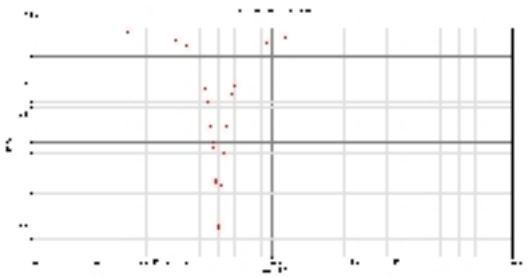

Fig. 5: Simulated S11 (input return loss)

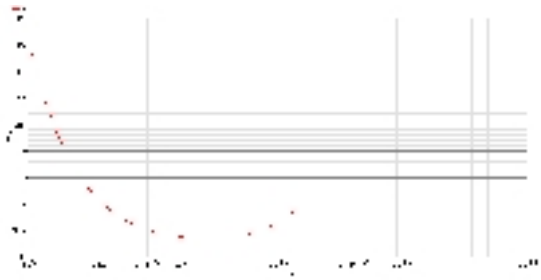

Fig. 6: Stability factor

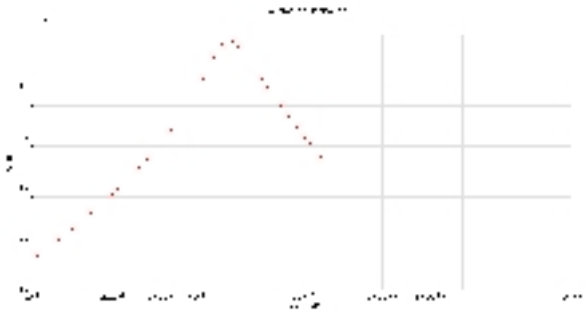

Fig. 7: Simulated S21

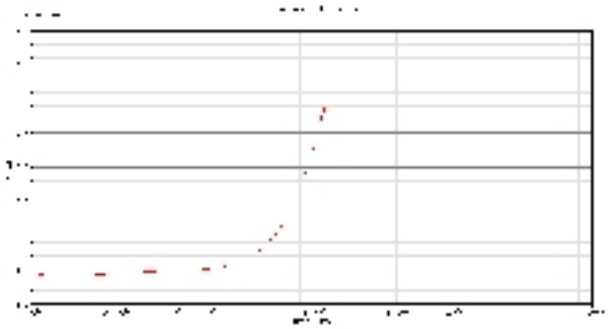

Fig. 8: Simulated Minimum Noise Fig.ure (NFmin)

S11also known as input return loss or input refection coefficient defined how much incident power is reflected back to the source from the amplifier. As shown in the Fig. 5 the value of S11 is -35dB for 6 GHz. The LNA is consider to be unconditionally stable if stability factor (K)>1 and Δ<1.And for this LNA, K=3.5 as shown in Fig. 6.The simulated values of S21 (power gain) is 19.8dB and F_{min} is 1.55dB which is shown in Fig. 7 and Fig. 8 respectively.

Table 3: Performance Summary of LNA

Parameter	Value
Technology	0.18 µm CMOS
Frequency	6 GHz
Min NF	1.55 dB
S11	-35 dB
Gain	19.8dB

The result of the proposed LNA is shown in table 3. At 6GHz, it has a min NF of 1.55 dB, gain of 19.8dB, and input return loss of -35 dB. In order to obtain low F_{min} , cascode configuration with inductive source degeneration is used. This is because source degenerated inductance will bring optimum noise impedance. The designed LNA requires only a 1.8V supply voltage and consumes10.8mW.

4. Conclusion

Particle Swarm Optimization (PSO) technique is used to design an optimized cascade LNA with inductive source degeneration in this paper. The design LNA is simulated in UMC 0.18µm CMOS technology. The designed inductive source degeneration cascode LNA exhibit features like low min noise figure, high voltage gain and low power dissipation. The main approach of this paper is to develop a methodology which reduces the noise of a LNA by making it independent on the details various noise mechanism

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References

A van der Ziel, Noise in Solid State Devices and Circuits. New York: Wiley 1086, ch.5

B. Razavi, (1997).RF Microelectronics, Prentice-Hall PTR.

Chan FTS, Tiwari MK. Swarm (2007).Intelligence: focus on ant and particle swarm optimization Vienna: I-Tech Education and Publishing,.

Chan, F. T. S., & Tiwari,M. K. (2007). Swarm Intelligence: focus on ant and particle swarm optimization. Vienna: I-Tech Education and Publishing.

Clerc, M. (2006). Particle swarm optimization, International scientific and technical encyclopedia

D. K. Shaeffer and T. H. Lee (1997).“A 1.5-V, 1.5-GHz CMOS low noise amplifier,” IEEE J. Solid-State Circuits, vol. 32, pp. 745–759, May

David J. Allstot, Xiaoyong Li, and SudipShekhar,(2004) “Design considerations for CMOS low-noise amplifiers,” symp. IEEE on RFIC, pp.97-100.

Fakhfakh M, Cooren Y, Sallem A, Loulou M, Siarry P,(2010).Analog circuit design optimization through the particle swarm optimization technique. Analog Integrated Circuits and Signal Processing, 63: 71–82.

Graeb, H., Zizala, S., Eckmueller, J., &Antreich, K. (2001). The sizing rules method for analog integrated circuit design. IEEE/ACM International conference on computer-aided design,

K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng,(1990). “A physics-based MOSFET noise model for circuit simulators,” *IEEE Trans. Electron Devices*, vol. 37, pp. 1323–1333.

Kennedy J., Eberhart R. Particle Swarm Optimization. *Proc. of IEEE Intl. Conf. Neural Networks Piscataway NJ 1995*, 1942-1948.

Scholten, A.J., Tiemeijer, L.F., Langevelde, R.V., Havens, R.J.,Duijnhoven, A.T.A.Z.V., and Venezia, V.C.(2003): ‘Noise modeling for RF CMOS circuit simulation’, IEEE Trans. Electron Devices, , 50,(5), pp. 618–632

T. H. Lee,(2002) “5-GHz CMOS wireless LANs,” IEEE Trans. Microwave Theory Tech., vol. 50, pp. 268–280, Jan.

T. Manku, M. Obrecht, and Y. Lin, (1999). “RF simulations and physics of the channel noise parameters within MOS transistors,” presented at the Proc. IEEE Custom Integrated Circuits Conf., paper 16-2.

The Design of CMOS Radio Frequency Integrated Circuits. Cambridge, U.K.: Cambridge Univ. Press, 1998

Toumazou, C., Lidgey, F. J., & Haigh, D. G. (1993). Analog integrated circuits: The current mode approach, IEEE circuit and systems series 2.